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NOISE-AWARE DATA PRESERVING SEQUENTIAL MTCMOS CIRCUITS WITH DYNAMIC FORWARD BODY BIAS

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Multi-threshold voltage CMOS (MTCMOS) is the most widely used circuit technique for suppressing the subthreshold leakage currents in idle circuits. When a conventional sequential MTCMOS circuit transitions from the sleep mode to the active mode, significant bouncing noise is produced on the power and ground distribution networks. The reliability of the surrounding active circuitry is seriously degraded. A dynamic forward body bias technique is proposed in this paper to alleviate the ground bouncing noise in sequential MTCMOS circuits without sacrificing the data retention capability. With the new dynamic forward body bias technique, the peak ground bouncing noise is reduced by up to 91.70% as compared to the previously published sequential MTCMOS circuits in a UMC 80 nm CMOS technology. The design tradeoffs among important design metrics such as ground bouncing noise, leakage power consumption, active power consumption, data stability, and area are evaluated.

Keywords: Power gating; ground bouncing noise; data retention; tri-mode; threshold voltage tuning; leakage power consumption; flip-flop; shift register.

1. Introduction

The subthreshold leakage currents currently dominate the overall power consumption of state-of-the-art integrated circuits due to the aggressive scaling of CMOS technology over the years.[1] One of the commonly used subthreshold leakage power reduction strategies is MTCMOS (also known as power gating).[2] In an MTCMOS circuit, high threshold voltage (high-$|V_{\text{th}}|$) sleep transistors (header and footer) are used to cut off the power supply and/or the ground connection to the idle low threshold voltage (low-$|V_{\text{th}}|$) circuit blocks as shown in Fig. 1. Specialized MTCMOS circuit techniques exist to maintain the data while lowering the leakage power consumption in idle sequential circuits.[2–4,6,10,12]

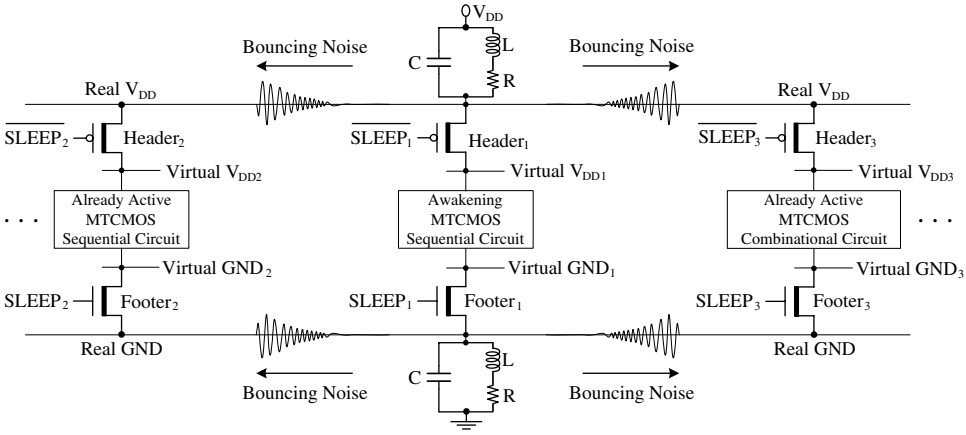

Fig. 1. A conventional multi-domain MTCMOS circuit with multiple autonomous low-$|V_{\text{th}}|$ circuit blocks with individual distributed sleep transistors. High-$|V_{\text{th}}|$ sleep transistors are represented with a thick line in the channel region. $\text{SLEEP}_1 : 0 \rightarrow V_{\text{DD}}$. $\text{SLEEP}_2 = \text{SLEEP}_3 = V_{\text{DD}}$.

Data reliability is an important concern in sequential MTCMOS circuits. When a typical sequential MTCMOS circuit transitions from the idle mode to the active mode, high instantaneous currents flow through the sleep transistors. Large voltage fluctuations occur on both the real power line (power bouncing noise) and the real ground distribution network (ground bouncing noise) as illustrated in Fig. 1. Bouncing noise generated in one power-gating domain during a wake-up event is transferred through the shared power and ground distribution networks to the surrounding active circuit blocks.[11] The node voltages and logic states of the active circuit blocks are thereby disturbed in a multi-domain MTCMOS circuit. The ground bouncing noise is expected to become an increasingly important reliability issue in future deeply scaled multi-domain MTCMOS integrated circuits with shrinking noise margins.[11] The development of novel noise-aware sequential MTCMOS circuits with low leakage data retention sleep mode capability is highly desirable.

In this paper, different sequential MTCMOS circuits with data retention capability are evaluated. A new dynamic forward body bias technique is explored to significantly suppress the ground bouncing noise produced by a sequential MTCMOS circuit during the sleep to active mode transitions. The attractive application space of different data preserving sequential MTCMOS circuit techniques is identified with a rigorous characterization of various important design metrics.

The paper is organized as follows. Previously published sequential MTCMOS circuit techniques with data retention capability are described in Sec. 2. The new dynamic forward body bias technique is introduced in Sec. 3 to reduce the ground bouncing noise produced during sleep to active mode transitions. Post-layout simulation results are presented in Sec. 4 to characterize the different data preserving sequential MTCMOS circuit techniques. Finally, the paper is concluded in Sec. 5.

2. Previously Published Data Retention MTCMOS Flip-Flops

Various specialized power gating techniques are published in the literature to maintain the data while reducing the leakage power consumption in idle sequential MTCMOS circuits.[2–4,6,10,12] These previously published sequential power gating techniques are reviewed in this section. The conventional Mutoh MTCMOS flip-flop is discussed in Sec. 2.1. The Balloon MTCMOS flip-flop is presented in Sec. 2.2. The standard zero-body-biased tri-mode MTCMOS flip-flop specifically targeting the ground bouncing noise issues in sequential MTCMOS circuits is described in Sec. 2.3.

2.1. *Conventional Mutoh MTCMOS flip-flop*

The Mutoh flip-flop (Mutoh-FF)[2,3] is the first-ever published MTCMOS FF with data retention capability. The circuit schematic is shown in Fig. 2. The Mutoh-FF provides a low-leakage sleep mode where the data is maintained in the master latch. Distributed and localized header and footer sleep transistors are utilized in the master and slave latches to eliminate the sneak leakage current paths. All of the devices along the critical path of the Mutoh-FF have low $|V_{\text{th}}|$ for maintaining similar Clock-to-Q speed as compared to a standard single low-$|V_{\text{th}}|$ FF. Although the Mutoh-FF is capable of maintaining the data while lowering the leakage power consumption, the circuit suffers from high area and active power consumption overheads as compared to the standard single low-$|V_{\text{th}}|$ FF.[22] Despite the significant area and active power overheads, Mutoh-FF has been widely used and referenced as an effective technique to lower leakage currents in idle sequential MTCMOS circuits.[2,3,8,10] The noise characteristics of the Mutoh-FF however have been overlooked and neglected until now. One of the important goals of this study is to evaluate the significance of the ground bouncing noise produced by the Mutoh-FF during the sleep to active mode transitions. As quantitatively shown in the following

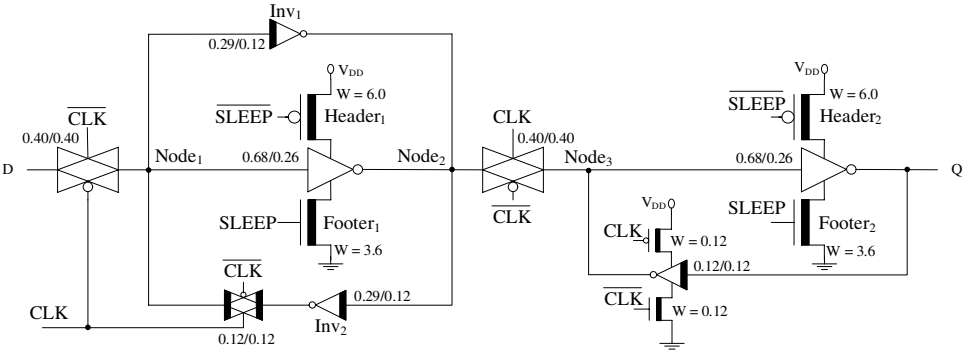

Fig. 2. The conventional MTCMOS flip-flop (Mutoh-FF) with data preserving sleep mode.[2,3] High-$|V_{\text{th}}|$ transistors are represented with a thick line in the channel region. The transistor sizes ($W_{\text{PMOS}}/W_{\text{NMOS}}$) are in micrometers assuming an 80 nm CMOS technology. All the channel lengths are minimum ($L = 80\,\text{nm}$).

sections, the commonly cited Mutoh-FF suffers from high ground bouncing noise, thereby seriously degrading the reliability of the surrounding active circuitry during the reactivation events.

2.2. *Balloon MTCMOS flip-flop*

An alternative MTCMOS flip-flop (Balloon-FF) for providing a high speed and low leakage data preserving sleep mode is presented in Ref. 4. A high-$|V_{\text{th}}|$ data retention cell (Balloon) is attached to the slave latch of the Balloon-FF as shown in Fig. 3. All of the devices on the forward and feedback paths have low $|V_{\text{th}}|$. The Clock-to-Q speed of the Balloon-FF is therefore similar to a standard single low-$|V_{\text{th}}|$ FF. A centralized NMOS sleep switch is employed for cutting the ground connection of the low-$|V_{\text{th}}|$ master and slave stages in the sleep mode with the Balloon-FF. Since only one centralized NMOS sleep transistor is employed, the circuit area and active power consumption overheads of Balloon-FF are reduced as compared to the Mutoh-FF. The Balloon-FF, however, requires two extra control signals B1 and B2. Furthermore, these two control signals have complex timing requirements for storing and retrieving the circuit state to and from the data retention balloon while entering and

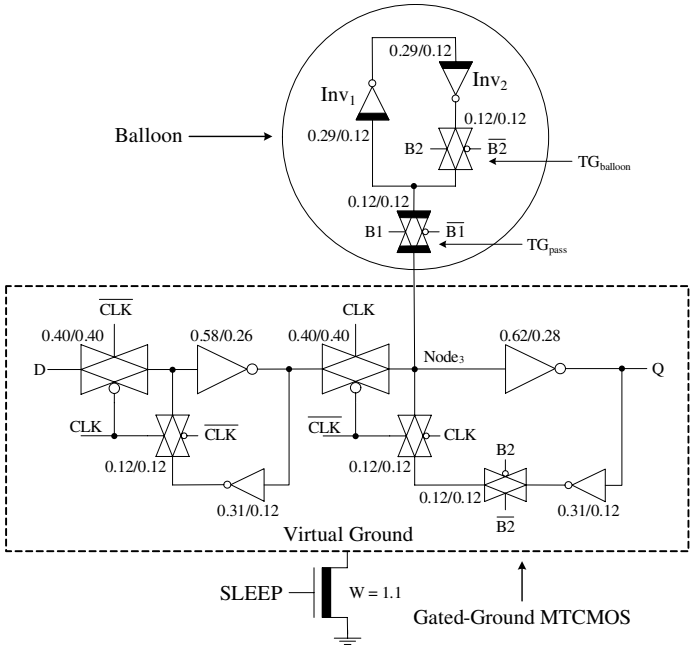

Fig. 3. Low-leakage Balloon MTCMOS flip-flop (Balloon-FF) with data preserving sleep mode.[4] High-$|V_{\text{th}}|$ transistors are represented with a thick line in the channel region. The transistor sizes ($W_{\text{PMOS}}/W_{\text{NMOS}}$) are in micrometers assuming an 80 nm CMOS technology. All the channel lengths are minimum ($L = 80$ nm).

leaving the sleep mode, respectively.[12;22] The Balloon-FF has a high energy overhead due to the complex data storage and recovery operations required for mode transitions. Furthermore, as quantitatively shown in the following sections, the Balloon-FF produces high ground bouncing noise due to the high voltage swing on the virtual ground line during the sleep to active mode transitions. The Balloon-FF thereby acts as an aggressor that imposes a potential reliability problem for the surrounding already active circuit blocks (see Fig. 1).

2.3. *Standard tri-mode MTCMOS flip-flop*

A specialized tri-mode power gating structure is proposed in Ref. 6 to lower the ground bouncing noise produced during the activation of idle MTCMOS circuits. All of the devices on the forward and feedback paths of a tri-mode FF have low $|V_{\text{th}}|$ as shown in Fig. 4. A high-$|V_{\text{th}}|$ PMOS data preserving transistor (Parker) is connected in parallel with the footer (N_1) to implement a low-leakage data retention sleep mode. The Parker is activated while N_1 is maintained cut-off (SLEEP = PARK = 0 V) during the sleep mode. The virtual ground line is maintained at the threshold voltage of the Parker ($|V_{\text{tp}}|$). The circuit is capable of lowering the leakage power consumption while retaining the data by maintaining a reduced yet significant voltage difference ($V_{\text{DD}} - |V_{\text{tp}}|$) between the power supply and the virtual ground line in the sleep mode. Since there are no extra data retention elements attached to the forward path, the parasitic capacitance on the critical path is smaller as compared to the Mutoh-FF and Balloon-FF. The Clock-to-Q speed of the tri-mode FF is therefore faster as compared to the Mutoh-FF and Balloon-FF.

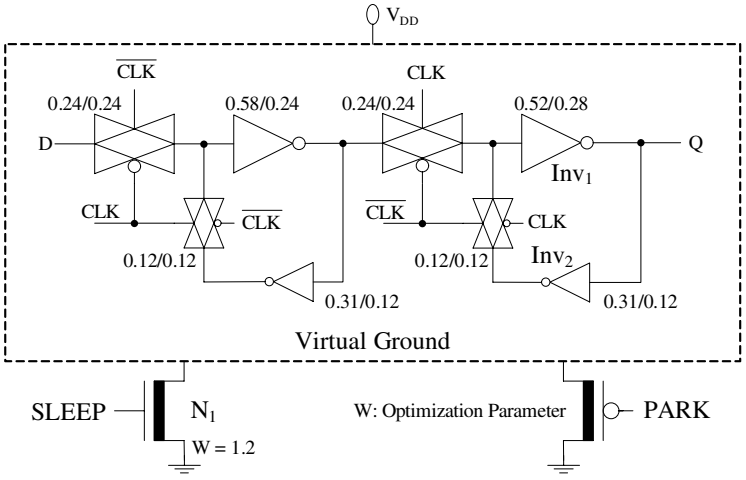

Fig. 4. Standard tri-mode MTCMOS flip-flop with zero-body-biased high-$|V_{\text{th}}|$ Parker (TMH).[6] High-$|V_{\text{th}}|$ transistors are represented with a thick line in the channel region. The transistor sizes ($W_{\text{PMOS}}/W_{\text{NMOS}}$) are in micrometers assuming an 80 nm CMOS technology. All the channel lengths are minimum ($L = 80$ nm).

A small-sized centralized footer (N_1) is used with the tri-mode circuit. The current produced by the smaller footer is reduced, thereby lowering the ground bouncing noise produced during the transitions from the data retention sleep mode to the active mode as compared to the Mutoh-FF. The ground bouncing noise produced by the tri-mode circuit is also suppressed due to the lower range of the voltage swing on the virtual ground line during the reactivation events as compared to the Balloon-FF.

In addition to offering a low-leakage data retention sleep mode, the tri-mode technique also provides an optional minimum leakage deep sleep mode.[10] When the data in idle sequential MTCMOS circuits are not required to be maintained, the tri-mode FF can transition to the alternative minimum leakage deep sleep mode (SLEEP = 0 and PARK = V_{DD}) where the data are lost.[10] Leakage savings are maximized by turning off the footer and the Parker in the deep sleep mode at the cost of losing the pre-sleep circuit state. In this paper, sleep mode data retention is assumed to be required in the sequential MTCMOS circuits. Therefore, the optional deep sleep mode provided by the tri-mode technique is not utilized in the following sections.

3. The New Dynamic-Forward-Body-Biased Tri-Mode MTCMOS Flip-Flop

A new design strategy based on threshold voltage tuning is described in this section to further suppress the ground bouncing noise produced during transitions from data retention sleep mode to active mode in sequential MTCMOS circuits. A dynamic-forward-body-biased noise-aware tri-mode MTCMOS circuit technique is proposed as shown in Fig. 5.

The high-$|V_{th}|$ Parker in the standard tri-mode circuit is substituted by a low-$|V_{th}|$ Parker as shown in Fig. 5(a). The threshold voltage of the Parker is further reduced by applying forward body bias. The steady-state sleep mode voltage on the virtual ground line of the tri-mode circuit with a forward-body-biased low-$|V_{th}|$ Parker is decreased, thereby reducing the voltage swing on the virtual ground line during the sleep to active mode transition as compared to the standard zero-body-biased tri-mode circuit. When the footer is turned on to resume the high performance active mode operations of the tri-mode circuit, the peak ground bouncing noise is suppressed with the proposed forward body bias technique. Furthermore, the data stability is enhanced by lowering the steady-state voltage of the virtual ground line in the sleep mode.

The previously published conventional forward body bias techniques[14–16] cannot be directly applied to the Parker since the virtual ground line voltage (the source of the Parker is attached to the virtual ground line) varies with the mode of operation of an MTCMOS circuit, the size of the Parker, and the size of the low-$|V_{th}|$ circuit block. A new forward body bias generator is therefore proposed in this paper. The circuit is shown in Fig. 5(b). A low-$|V_{th}|$ NMOS transistor (Biaser) and a negative DC voltage source (V_{bias}) are attached to the tri-mode circuit to produce a dynamically adjusted

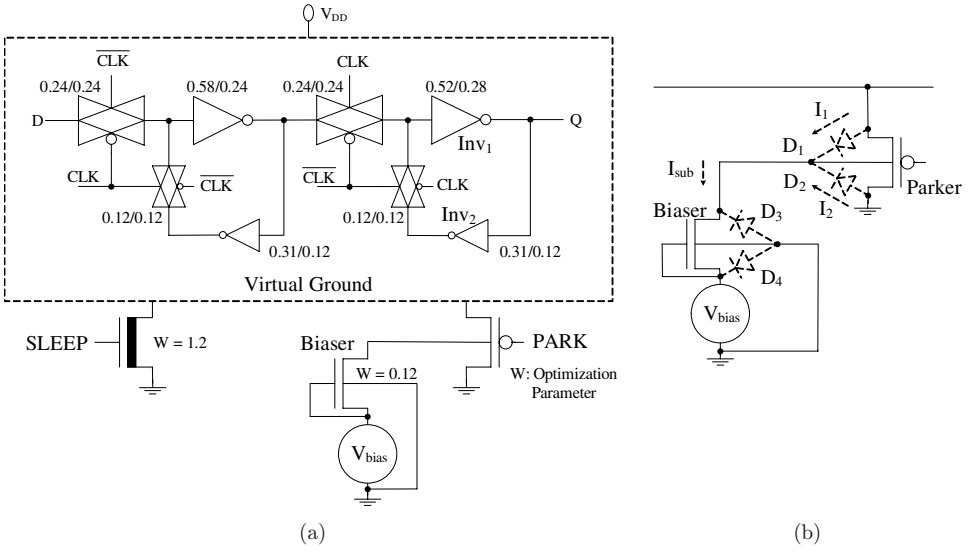

Fig. 5. Proposed sequential MTCMOS circuit with dynamic-forward-body-biased Parker (DFBB). (a) The tri-mode MTCMOS flip-flop with a dynamic-forward-body-biased low-$|V_{\text{th}}|$ Parker (DFBBL). (b) The proposed dynamic forward body bias generator for the Parker. High-$|V_{\text{th}}|$ transistors are represented with a thick line in the channel region. The transistor sizes ($W_{\text{PMOS}}/W_{\text{NMOS}}$) are in micrometers assuming an 80 nm CMOS technology. All the channel lengths are minimum ($L = 80\,\text{nm}$).

body voltage for the Parker. The Biaser is maintained cut-off by shorting the gate and the source terminals. The drain current of the Biaser controls the body current of the Parker. The body current of the Parker is primarily composed of the currents produced by D_1 (I_1) and D_2 (I_2) as illustrated in Fig. 5(b). D_1 and D_2 are the source-to-body and drain-to-body p−n junctions, respectively, of the Parker.

During the sleep mode, the virtual ground line is charged to $|V_{\text{tp}}|$. The body of the Parker is maintained at a voltage level between $|V_{\text{tp}}|$ and V_{bias}. D_1 is forward biased. During the subsequent active mode, the virtual ground line is discharged to $\sim V_{\text{gnd}}$. The body of the Parker is maintained at a voltage level between V_{gnd} and V_{bias}. Both D_1 and D_2 are forward biased. The Parker thereby experiences continuous forward body bias in both sleep and active modes with the proposed technique.

The subthreshold leakage current (I_{sub}) produced by the Biaser and the body voltage of the Parker are determined by V_{bias}. I_{sub} is

$$I_{\text{sub}} = I_1 + I_2\,. \tag{1}$$

The body voltage of the Parker is dynamically adjusted by the body bias generator to satisfy Eq. (1) during the different modes of operation. The forward body bias voltage of the Parker is tuned by adjusting V_{bias}. Higher I_{sub} enhances the forward body bias voltage experienced by the Parker, thereby lowering the ground bouncing noise as well as strengthening the data stability. Higher I_{sub}, however, also increases the

leakage power consumption in the sleep mode. The leakage power consumption of the tri-mode circuit can be restricted to an acceptably low level by choosing an appropriate V_{bias} as further discussed in the following sections.

4. Simulation Results

The UMC 80 nm multi-threshold voltage CMOS technology[17] (high-$V_{th\_NMOS} = 370$ mV, low-$V_{th\_NMOS} = 155$ mV, high-$V_{th\_PMOS} = -310$ mV, low-$V_{th\_PMOS} = -105$ mV, and $V_{DD} = 1$ V) is used in this paper for the characterization of ground bouncing noise, leakage power consumption, active power consumption, data stability, and area overheads with the different sequential MTCMOS techniques. Five 32-bit shift registers are designed based on the following techniques: standard single low-$|V_{th}|$ FF, the conventional Mutoh-FF (Fig. 2), the Balloon-FF (Fig. 3), the standard zero-body-biased tri-mode technique (TMH in Fig. 4), and the dynamic-forward-body-biased tri-mode technique (DFBBL in Fig. 5). All the data presented in this section are produced by post-layout simulation with Synopsys HSPICE.[19] The layouts are drawn with Cadence Virtuoso.[20] 2D parasitic RC extraction of the layouts is performed with Cadence Assura.[21]

The design criterion used in this paper for the sizing of sleep transistors is to achieve similar propagation delays (within 5%) with each flip-flop and shift register. The load and the driver used for propagation delay measurements are identical flip-flops (for example, a standard single low-$|V_{th}|$ flip-flop driving an identical standard single low-$|V_{th}|$ flip-flop or a TMH flip-flop driving an identical TMH flip-flop). The input data slew and clock slew are 50 ps for each flip-flop. The low-$|V_{th}|$ circuitry of each FF is carefully sized to achieve similar output rise and fall times as well as similar high-to-low and low-to-high propagation delays. The low-$|V_{th}|$ segments of the Mutoh-FF and Balloon-FF are also sized larger (in addition to appropriate sleep transistor sizing) to meet the timing requirement as compared to the standard single low-$|V_{th}|$ FF. The sizes of different MTCMOS FFs to satisfy the timing criterion with this UMC 80 nm CMOS technology are shown in Figs. 2–5. The sizes of sleep transistors used with different MTCMOS FFs and MTCMOS shift registers are listed in Table 1. The mutually exclusive switching patterns (the data in the adjacent flip-flops of the shift registers never switch in the same direction) are exploited to further reduce the sizes of the sleep transistors in the Balloon, TMH, and DFBBL shift

Table 1. The sizes of sleep transistors with different techniques.

	Flip-flop		Shift register	
Circuit technique	Header (μm)	Footer (μm)	Header (μm)	Footer (μm)
Mutoh	12.0	7.2	384.0	230.4
Balloon	N/A	1.1	N/A	17.6
TMH	N/A	1.2	N/A	19.2
DFBBL	N/A	1.2	N/A	19.2

registers.[7] Alternatively, sleep transistors of different FFs in the Mutoh shift register cannot be shared. Localized and distributed sleep transistors are required in order to eliminate the sneak leakage current paths in Mutoh-FF.[22] Different tapered buffer chains are employed to provide similar signal rise and fall times to the sleep transistors and the clock distribution network with each technique.

Section 4 is organized as follows. The ground bouncing noise produced by different sequential MTCMOS circuits during the sleep to active mode transitions is evaluated in Sec. 4.1. The leakage power consumed by different shift registers is compared in Sec. 4.2. The active power consumption of the shift registers are presented in Sec. 4.3. The area overheads of the MTCMOS shift registers are compared in Sec. 4.4. The data stabilities of the MTCMOS FFs in the sleep mode are evaluated in Sec. 4.5. A comprehensive design metric is proposed in Sec. 4.6 to compare the overall electrical quality of data preserving sequential MTCMOS shift registers.

4.1. *Ground bouncing noise*

The ground bouncing noise produced by the sequential MTCMOS circuits is characterized in this section. The commonly used and well characterized 40-pin Dual In-line Package (DIP-40) model is used in this paper to evaluate the ground bouncing noise phenomenon in sequential MTCMOS circuits. The parasitic resistance, inductance, and capacitance of the DIP-40 are 217 mΩ, 8.18 nH, and 5.32 pF, respectively.[5,10,12,18]

In order to evaluate the tradeoffs between ground bouncing noise and leakage power consumption with the TMH and DFBBL techniques, the width of the Parker is varied from the minimum size allowed by the technology (0.12 μm) to 15 μm. Furthermore, V_{bias} in the DFBBL circuit is swept from 0 V to -700 mV to evaluate the dependence of ground bouncing noise on the value of V_{bias}. When $V_{\text{bias}} = 0$ V, the gate and source of the Biaser are directly connected to the ground. The additional voltage reference within the body bias generator is thereby eliminated. While the Parker is forward-body-biased even with $V_{\text{bias}} = 0$ V, to be able to produce higher forward body bias voltages that can further reduce the ground bouncing noise while enhancing the data stability with different Parker sizes, an additional nonzero voltage reference (V_{bias}) is required with the proposed body bias generator. The nonzero voltage reference V_{bias}, however, requires additional design effort and causes area overhead. The minimum applicable V_{bias} is assumed to be -700 mV[15,16] in this study to maintain the reliability of the Biaser (to avoid strong forward currents through the body diodes). The Biaser is sized minimum (0.12 μm) to lower the area overhead. The ground bouncing noise produced with different tri-mode circuits are shown in Figs. 6 and 7.

When the size of the Parker increases, the steady-state sleep-mode voltage of the virtual ground line with the tri-mode circuit decreases. The voltage swing on the virtual ground line is therefore reduced during the transition from the sleep mode to the active mode. The peak ground bouncing noise produced by different tri-mode

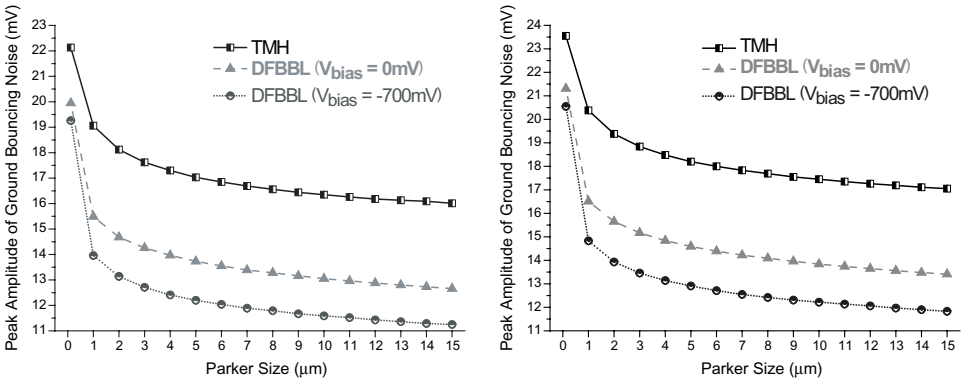

Fig. 6. The peak ground bouncing noise produced by the TMH and DFBBL shift registers with different Parker sizes. $T = 90°$C. (a) Stored data = "0". (b) Stored data = "1". The minimum Parker size on the X axis is 0.12 μm.

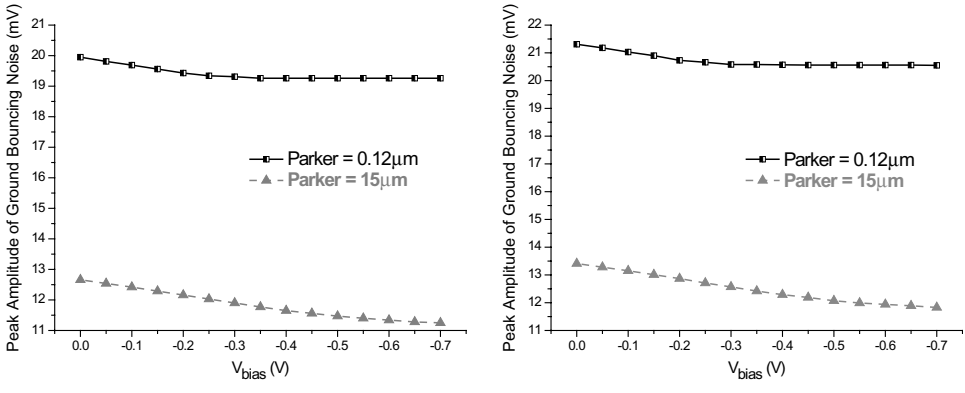

Fig. 7. The peak ground bouncing noise produced by the DFBBL shift register at different V_{bias}. $T = 90°$C. (a) Stored data = "0". (b) Stored data = "1".

circuits during the reactivation events thereby monotonically decreases with the increased Parker size as shown in Fig. 6.

I_{sub} (in Eq. (1)) is increased when V_{bias} is decreased from 0 mV to −700 mV, thereby enhancing the forward body bias voltage experienced by the Parker in the DFBBL circuit. The threshold voltage of the Parker is therefore reduced with the decreased V_{bias}. The peak ground bouncing noise produced by the DFBBL circuit monotonically decreases with the reduced V_{bias} due to the suppressed voltage swing on the virtual ground line during the sleep to active mode transition as shown in Fig. 7.

The peak amplitudes of the ground bouncing noise induced on the real ground distribution network with different MTCMOS circuit techniques are listed in Table 2.

Table 2. Peak amplitudes (mV) of ground bouncing noise with different MTCMOS techniques.

Circuit technique	Stored data: 0	Stored data: 1
Mutoh	135.47	134.74
Balloon	66.97	60.69
TMH	16.01−22.13	17.05−23.55
DFBBL	11.25−19.95	11.83−21.31

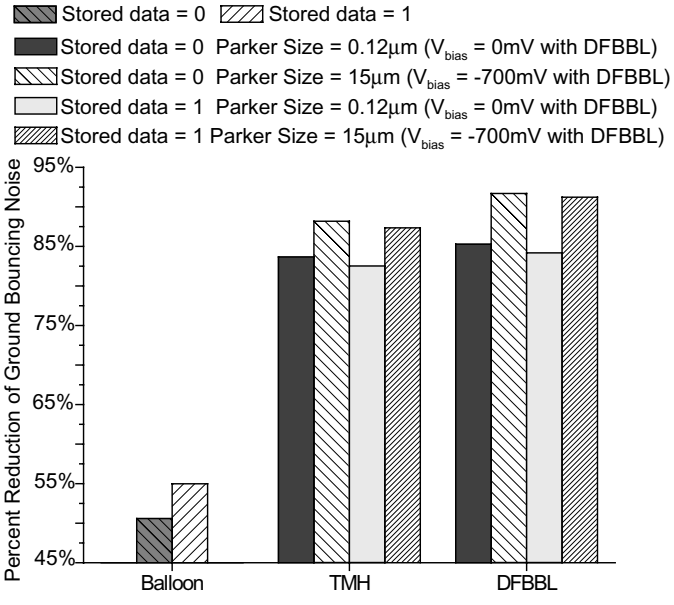

Fig. 8. Percent reduction of ground bouncing noise produced with different MTCMOS circuit techniques as compared to the conventional Mutoh technique at 90°C.

The percent reductions of ground bouncing noise produced with different circuit techniques as compared to the Mutoh shift register are shown in Fig. 8. The simulation temperature is 90°C. The Mutoh shift register is used as a worst-case reference since the highest ground bouncing noise is produced by the Mutoh shift register among the sequential MTCMOS circuits evaluated in this paper. The total size of the sleep transistors is significantly larger in the Mutoh shift register as compared to the other MTCMOS circuit techniques. The Mutoh shift register therefore produces higher instantaneous currents and more significant noise during the transitions from the sleep mode to the active mode.

The DFBBL shift register achieves the lowest ground bouncing noise among the MTCMOS techniques evaluated in this paper due to the suppressed voltage swing on the virtual ground line with the proposed threshold voltage tuning strategy. The peak ground bouncing noise is reduced by up to 91.70% and 83.20% as compared to

the Mutoh and Balloon shift registers, respectively. Furthermore, the DFBBL shift register reduces the peak ground bouncing noise by up to 30.62% as compared to the TMH shift register with the same Parker size.

4.2. *Leakage power consumption*

The leakage power consumption of the 32-bit shift registers designed with different circuit techniques are evaluated in this section. The majority of the MTCMOS circuits evaluated in this paper utilize the modified gated-ground technique. The virtual ground and the internal nodes of a gated-ground MTCMOS circuit have high steady-state voltages in the low leakage data retention sleep mode. A high data input ($D = V_{\mathrm{DD}}$) is therefore assumed for the leakage power measurements. The data stored in each flip-flop of the shift registers are assumed to be the same (either all "0" or all "1"). The leakage power consumption with the TMH and DFBBL shift registers are shown in Figs. 9 and 10. The simulation temperature is 90°C.

The Parkers in the TMH and DFBBL shift registers are turned on to maintain a reduced yet significant voltage difference between the power and ground connections of the low-$|V_{\mathrm{th}}|$ sequential circuits in the data retention sleep mode. The leakage power consumed by the TMH and DFBBL shift registers are therefore determined by the effective supply voltage experienced by the low-$|V_{\mathrm{th}}|$ sequential circuits and the size of the Parker. When the size of the Parker is increased, the steady-state sleep-mode voltage of the virtual ground line is reduced, thereby enhancing the effective supply voltage experienced by the low-$|V_{\mathrm{th}}|$ sequential circuits. Higher drain current is produced by the active Parker, thereby increasing the leakage power consumption in the sleep mode as shown in Fig. 9.

The steady-state sleep-mode voltage of the virtual ground line is reduced with the decreased V_{bias} in the DFBBL shift register as discussed in Sec. 4.1. The effective

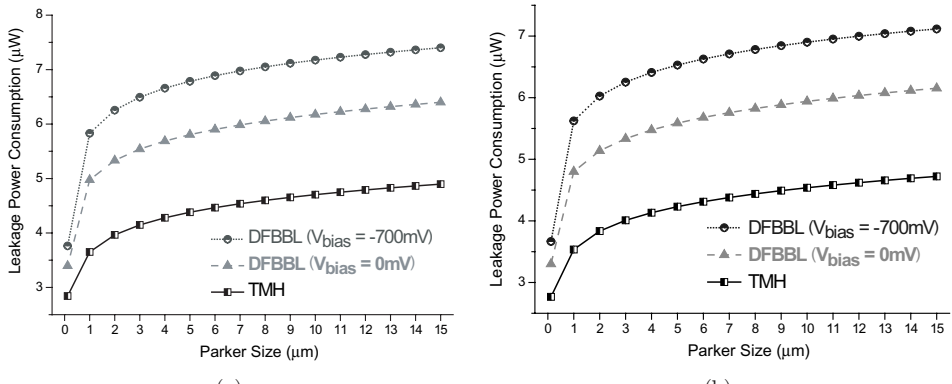

Fig. 9. The leakage power consumed by the TMH and DFBBL shift registers with different Parker sizes. $T = 90°\mathrm{C}$. (a) Stored data = "0". (b) Stored data = "1". The minimum Parker size on the X axis is 0.12 μm.

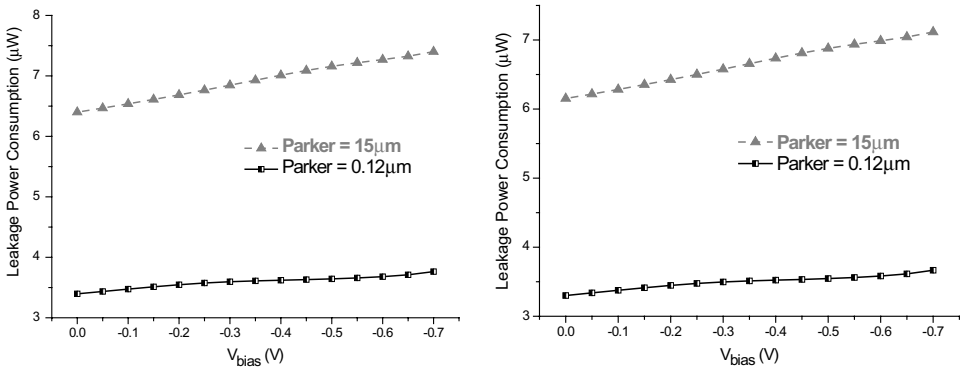

Fig. 10. The leakage power consumed by the DFBBL shift register at different V_{bias}. $T = 90°\text{C}$. (a) Stored data = "0". (b) Stored data = "1".

supply voltage experienced by the low-$|V_{\text{th}}|$ sequential circuits is thereby enhanced. Furthermore, the body diode currents of the Parker and Biaser are increased as V_{bias} is reduced. The leakage power consumption of the DFBBL shift register therefore monotonically increases with decreased V_{bias} as shown in Fig. 10.

The leakage power consumed by different shift registers is listed in Table 3. The percent leakage power reductions provided by different MTCMOS circuit techniques in the data retention sleep mode (as compared to the standard single low-$|V_{\text{th}}|$ shift register) are shown in Fig. 11. As listed in Table 3, the DFBBL shift register consumes the highest leakage power (among MTCMOS circuits) due to the highest drain current through the active Parker and the high body diode currents of the Parker and the body bias generator. The DFBBL shift register increases the leakage power consumption by 3.16× to 7.57× and 7.26× to 16.25× as compared to the Mutoh and Balloon shift registers, respectively, depending on the stored data, the size of the Parker, and the value of V_{bias}. Furthermore, the DFBBL shift register increases the

Table 3. Leakage power consumption (μW) of different shift registers.

Circuit technique	Stored data: 0	Stored data: 1
Standard single low-$\|V_{\text{th}}\|$	15.468	15.616
Mutoh	1.073	0.940
Balloon	0.468	0.438
TMH	2.842−4.897	2.767−4.722
DFBBL	3.396−7.401	3.300−7.116

Note: The minimum and the maximum leakage power consumption with the TMH circuit are observed when the Parker size is 0.12 μm and 15 μm, respectively. The minimum and the maximum leakage power consumption with the DFBBL circuit are observed when the Parker size is 0.12 μm with $V_{\text{bias}} = 0\,\text{mV}$ and the Parker size is 15 μm with $V_{\text{bias}} = -700\,\text{mV}$, respectively.

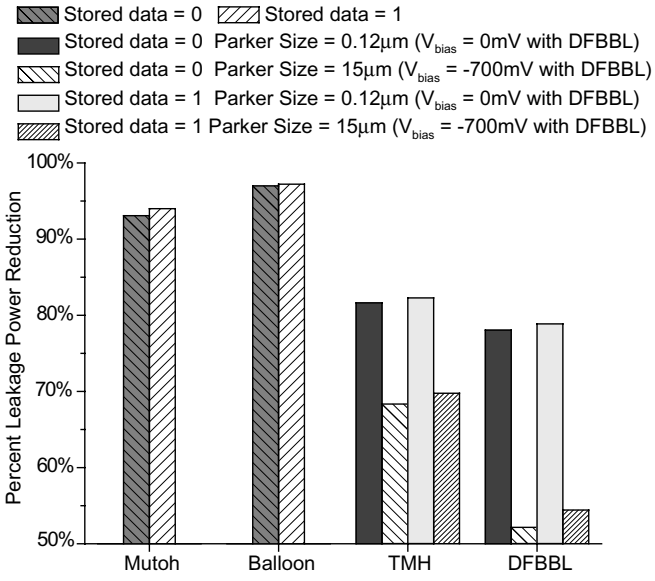

Fig. 11. Percent leakage power reduction provided by different MTCMOS circuit techniques in the sleep mode as compared to the standard single low-$|V_{\text{th}}|$ shift register.

leakage power consumption by up to 1.65 × as compared to the TMH shift register with the same Parker size. However, as compared to the standard single low-$|V_{\text{th}}|$ shift register, the DFBBL shift register manages to suppress the leakage power consumption by 52.15%−78.87% as shown in Fig. 11. The DFBBL technique thereby maintains the effectiveness in suppressing the leakage power consumption as compared to the standard single low-$|V_{\text{th}}|$ shift register in the sleep mode.

Alternatively, the Balloon shift register consumes the lowest leakage power among the MTCMOS shift registers evaluated in this paper. As listed in Table 3, the Balloon shift register reduces the leakage power consumption by up to 97.20%, 93.84%, 90.72%, and 56.38% as compared to the standard single low-$|V_{\text{th}}|$, DFBBL, TMH, and Mutoh shift registers, respectively.

4.3. *Active power consumption*

The active power consumption with different shift registers is evaluated in this section. The clock frequency is 2 GHz. The simulation temperature is 90°C. The active power consumed by different shift registers is listed in Table 4. The normalized (with respect to the active power consumed by the Mutoh shift register) active power consumption with different circuit techniques are shown in Fig. 12.

The Mutoh-FF and Balloon-FF employ additional transistors and circuitry for implementing a low leakage data retention sleep mode. Furthermore, for similar speed, the transistors in the Mutoh-FF and Balloon-FF are sized larger as compared

Table 4. Active power consumption (mW) of different shift registers.

Circuit technique	Active power
Standard single low-$\|V_{th}\|$	1.624
Mutoh	3.062
Balloon	2.509
TMH	1.314
DFBBL	1.314

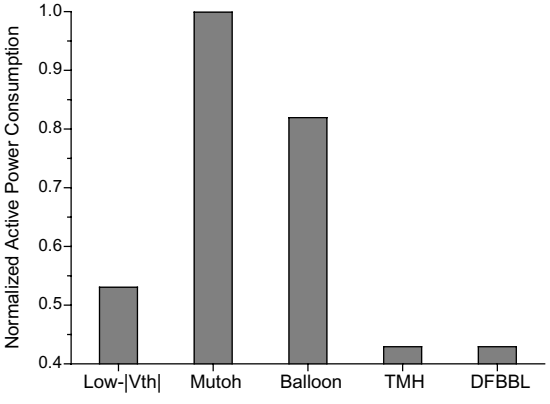

Fig. 12. The active power consumption with different circuit techniques normalized to the Mutoh shift register. $T = 90°C$.

to the standard single low-$|V_{th}|$ FF. The active power consumption is therefore increased by the Mutoh and Balloon MTCMOS techniques as compared to the standard single low-$|V_{th}|$ circuit as listed in Table 4. Alternatively, only an additional Parker is utilized in the tri-mode circuits to maintain the data in the sleep mode. Since the Parker is cut-off in the active mode, the influence of Parker size (as well as the body bias generator in the DFBBL circuit) on the active power consumption is small. The transistor sizes in the tri-mode FF do not change significantly as compared to the standard single low-$|V_{th}|$ FF. Due to the resistive voltage drop across the sleep transistors, the effective supply voltage experienced by the low-$|V_{th}|$ circuitry in the tri-mode shift register is lower as compared to the standard single low-$|V_{th}|$ shift register, thereby consuming less active power as listed in Table 4.[11]

The TMH and DFBBL shift registers consume the lowest active power among the different shift registers evaluated in this paper. The TMH and DFBBL shift registers reduce the active power consumption by 57.09%, 47.63%, and 19.09% as compared to the Mutoh, Balloon, and standard single low-$|V_{th}|$ shift registers, respectively. Alternatively, the Mutoh shift register consumes the highest active power among the different shift registers evaluated in this paper. With the Mutoh shift register, the

active power consumption is increased by 2.33×, 2.33×, 1.89×, and 1.22×, as compared to the TMH, DFBBL, standard single low-$|V_{\text{th}}|$, and Balloon shift registers, respectively.

4.4. *Area comparison*

The layout area comparison of different shift registers is provided in this section. The layout areas are listed in Table 5. The area overheads of different MTCMOS circuit techniques as compared to the standard single low-$|V_{\text{th}}|$ shift register are shown in Fig. 13. In this study, the additional DC voltage source V_{bias} in the DFBBL shift register is assumed to be already available in the power management unit on chip. Therefore, the overhead of V_{bias} is not taken into consideration.

The TMH and DFBBL shift registers have the lowest area overhead due to small centralized sleep transistors and the simplest control circuitry among the MTCMOS circuits evaluated in this paper. The TMH and DFBBL shift registers reduce the area

Table 5. Area (μm^2) of different shift registers.

Circuit technique	Area
Standard single low-$\|V_{\text{th}}\|$	633
Mutoh	1865
Balloon	1264
TMH	745−771
DFBBL	745−774

Note: The minimum and the maximum areas with the TMH and DFBBL circuits are reported for the Parker sizes of 0.12 μm and 15 μm, respectively.

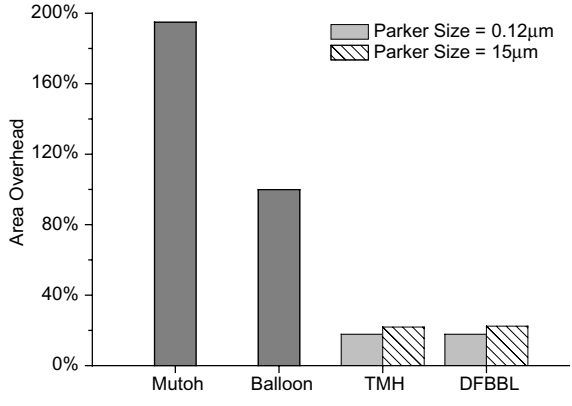

Fig. 13. The area overhead with different MTCMOS circuit techniques as compared to the standard single low-$|V_{\text{th}}|$ shift register.

by 60.09% and 41.12% as compared to the Mutoh and Balloon shift registers, respectively. Alternatively, the Mutoh-FF has the highest area overhead due to the distributed bulky sleep transistors and the huge buffer chains driving the sleep transistors. The Mutoh shift register increases the area by 2.95 ×, 2.51 ×, 2.51 ×, and 1.48 × as compared to the standard single low-$|V_{\text{th}}|$, TMH, DFBBL, and Balloon shift registers, respectively. The Balloon shift register also suffers from high area overhead due to the complicated control circuitry as shown in Fig. 13. Isolated additional buffer chains produce the multiple control signals required for the operation of the Balloon shift register, thereby further increasing the area overhead as compared to the TMH and DFBBL shift registers.

4.5. *Hold static noise margin of MTCMOS flip-flops*

The hold static noise margin (SNM) is the metric used to characterize the data stability of flip-flops in the low-leakage data retention sleep mode.[13] The hold static noise margins of the TMH and DFBBL FFs are shown in Figs. 14 and 15. The hold static noise margins of different MTCMOS FFs are listed in Table 6. The normalized (with respect to the hold SNM of the Balloon-FF) hold static noise margins of different MTCMOS FFs are shown in Fig. 16. The simulation temperature is 90°C.

The hold SNMs of the tri-mode circuits are determined by the voltage transfer characteristics (VTC) of the low-$|V_{\text{th}}|$ cross-coupled inverters (Inv_1 and Inv_2) in Figs. 4 and 5. Higher effective supply voltage experienced by the cross-coupled inverters enhances the hold SNM of the tri-mode circuits. As discussed in Sec. 4.2, the effective supply voltage experienced by the cross-coupled inverters is enhanced with

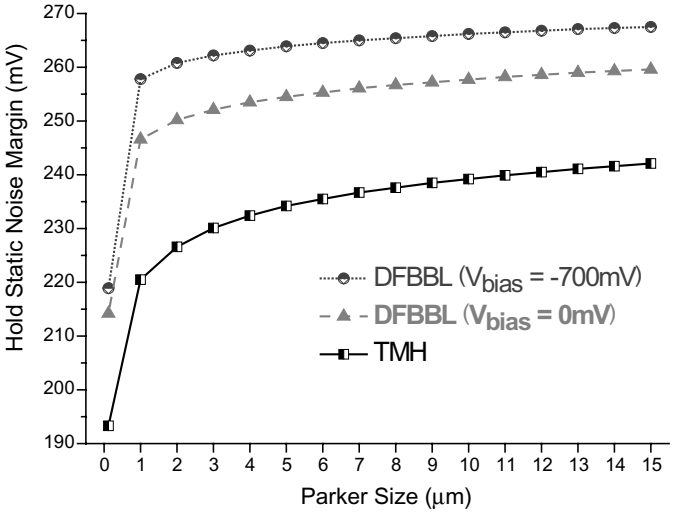

Fig. 14. The hold static noise margins of the TMH and DFBBL flip-flops with different Parker sizes. $T = 90°\text{C}$. The minimum Parker size on the X axis is 0.12 μm.

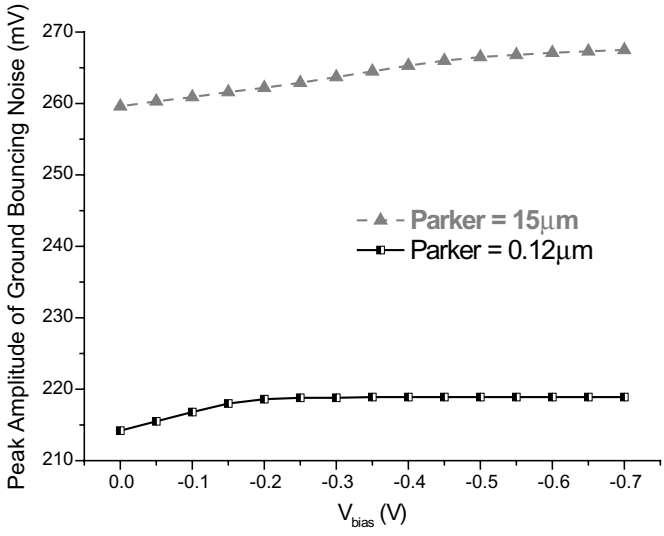

Fig. 15. The hold static noise margins of the DFBBL shift register at different V_{bias}. $T = 90°\text{C}$.

Table 6. Hold static noise margin (mV) of different flip-flops.

Circuit technique	90°C
Mutoh	357.1
Balloon	359.2
TMH	193.3−244.0
DFBBL	214.2−267.5

Note: The minimum and the maximum hold SNM with the TMH circuit are observed when the Parker size is 0.12 μm and 15 μm, respectively. The minimum and the maximum hold SNM with the DFBBL circuit are observed when the Parker size is 0.12 μm with $V_{\text{bias}} = 0\,\text{mV}$ and the Parker size is 15 μm with $V_{\text{bias}} = -700\,\text{mV}$, respectively.

the increased Parker size, thereby enhancing the hold SNM of the tri-mode circuit as shown in Fig. 14. Similarly, when V_{bias} (in the DFBBL circuit) is reduced, the effective supply voltage experienced by the cross-coupled inverters is increased. The hold SNM of the DFBBL FF is thereby enhanced with a smaller V_{bias} as shown in Fig. 15.

Alternatively, the hold SNMs of the Mutoh-FF and Balloon-FF are determined by the VTC of the high-$|V_{\text{th}}|$ cross-coupled inverters Inv_1 and Inv_2 in Figs. 2 and 3. The VTC of the high-$|V_{\text{th}}|$ cross-coupled inverters have narrower transition regions, thereby enhancing the hold SNM as compared to the low-$|V_{\text{th}}|$ inverters. Furthermore,

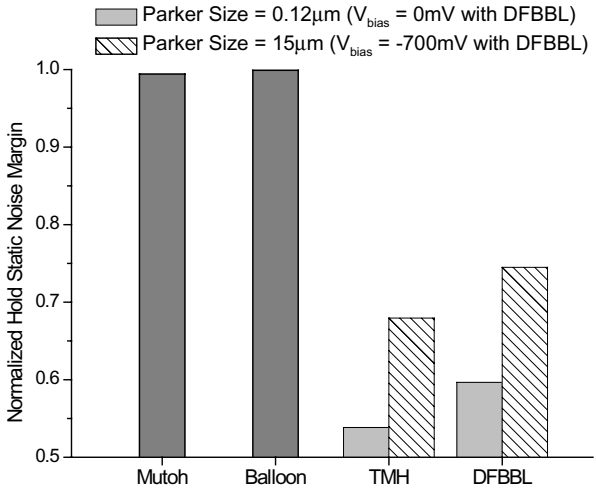

Fig. 16. The hold static noise margins of different MTCMOS circuit techniques normalized to the hold SNM of the Balloon-FF. $T = 90°C$.

since the power and ground of Inv_1 and Inv_2 in the Mutoh-FF and Balloon-FF are connected to the real power and ground networks (full V_{DD} experienced without any voltage degradation on sleep transistors), the hold SNMs are higher as compared to the TMH and DFBBL FFs. As listed in Table 6, the Balloon-FF achieves the highest hold SNM among the MTCMOS FFs evaluated in this paper. The hold SNM is enhanced by up to 85.83%, 67.69%, and 0.58% with the Balloon-FF as compared to the TMH, DFBBL, and Mutoh FFs, respectively. Alternatively, the TMH FF has the lowest hold SNM due to the low $|V_{th}|$ transistors and the lowest effective supply voltage of the cross-coupled data retention inverters. The hold SNM is enhanced by up to 16.92% with the DFBBL FF as compared to the TMH FF with the same Parker size.

4.6. *Electrical quality metric*

As discussed in the previous sections and as listed in Table 7, different sequential MTCMOS circuit techniques rank differently for various design metrics.

Table 7. Performance comparison of different data preserving sequential MTCMOS circuit techniques.

Primary design metric	Best technique	Worst technique
Ground Bouncing Noise	DFBBL	Mutoh
Leakage Power Consumption	Balloon	DFBBL
Active Power Consumption	TMH/DFBBL	Mutoh
Area	TMH/DFBBL	Mutoh
Data Stability	Balloon	TMH
Quality Metric	DFBBL	Mutoh

A comprehensive design metric is evaluated in this section to characterize the overall electrical *quality* of the different sequential MTCMOS circuit techniques. The Quality Metric is

$$\text{Quality Metric} = \frac{\text{Percent\_Leakage\_Power\_Reduction} \times \text{Hold\_SNM}}{\text{Ground\_Bouncing\_Noise} \times \text{Active\_Power} \times \text{Area}}, \qquad (2)$$

where percent leakage power reduction is calculated with respect to the standard single low-$|V_{\text{th}}|$ shift register. Based on this Quality Metric, the proposed DFBBL is identified as the most preferable circuit technique among the different sequential MTCMOS circuits evaluated in this paper. Alternatively, the Mutoh circuit technique has the lowest overall electrical *quality*. The Quality Metric is increased by 19.24 × to 28.24 × and 4.84 × to 7.10 × with the DFBBL circuit technique as compared to the Mutoh and Balloon circuits, respectively. Furthermore, the DFBBL circuit technique enhances the Quality Metric by up to 31% as compared to the conventional zero-body-biased tri-mode MTCMOS circuit with the same Parker size.

5. Conclusions

A novel threshold voltage tuning methodology is proposed in this paper to suppress the ground bouncing noise in data preserving sequential MTCMOS circuits. A new forward body bias generator is proposed to dynamically tune the threshold voltage of the Parker during different modes of operation of noise-aware sequential MTCMOS circuits.

The new dynamic forward body biased tri-mode MTCMOS is identified as the most preferable circuit technique based on a comprehensive electrical *Quality Metric* comparison among various sequential MTCMOS circuits. The peak ground bouncing noise is reduced by up to 91.70% and 30.62% with the proposed threshold voltage tuning technique as compared to the previously published Mutoh-FF and standard zero-body-biased tri-mode MTCMOS circuits, respectively, with a UMC 80 nm CMOS technology. Furthermore, the data stability of sequential MTCMOS circuits is enhanced by 16.92% with the new dynamic forward body bias technique as compared to the conventional zero-body-biased tri-mode circuit. The forward body bias technique also lowers the active power consumption and reduces the area as compared to the previously published data preserving sequential MTCMOS circuits.

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