Robust FinFET Memory Circuits with P-Type Data Access Transistors for Higher Integration Density and Reduced Leakage Power

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A new six transistor (6T) SRAM cell with PMOS access transistors is proposed in this paper for reducing the leakage power consumption while enhancing the data stability and the integration density of FinFET memory circuits. With the proposed SRAM circuit, the voltage disturbance at the data storage nodes during a read operation is reduced by utilizing PMOS access transistors. The read stability is enhanced by up to 62% while reducing the leakage power by up to 22% as compared to a standard tied-gate FinFET SRAM cell with the same size transistors. One gate of each pull-up FinFET of the cross-coupled inverters is permanently disabled in order to achieve write-ability with minimum sized transistors. The proposed independent-gate FinFET SRAM circuit with P-type data access transistors reduces the idle mode leakage power, the write power, and the cell area by up to 62%, 16.5%, and 25.53%, respectively, as compared to a standard tied-gate FinFET SRAM cell sized for similar data stability in a 32 nm FinFET technology.

Keywords: SRAM, Leakage Power, Enhanced Read Stability, Bitline Leakage, Independent Gate Bias.

1. INTRODUCTION

Scaling is the primary thrust behind the advancement of CMOS technology. The increased sub-threshold and gate-dielectric leakage currents and the enhanced device sensitivity to process parameter fluctuations have become the primary barriers against further CMOS technology scaling into the sub-45 nm regime. The FinFET offers distinct advantages for simultaneously suppressing the sub-threshold and gate dielectric leakage currents as compared to the traditional single-gate MOSFETs. The three electrically coupled gates and the thin silicon body suppress the short-channel effects of a FinFET, thereby reducing the sub-threshold leakage current\textsuperscript{1,13}. The suppressed short-channel effects and the enhanced gate control over the channel (lower sub-threshold swing) permit the use of a thicker gate oxide in a FinFET as compared to a conventional single-gate transistor. The gate oxide leakage current of a FinFET is thereby significantly reduced. The thin body of a FinFET is typically undoped or lightly doped. The carrier mobility is therefore enhanced and the device variations due to doping fluctuations are reduced in a FinFET as compared to a single-gate bulk transistor. Successful fabrication of tied-gate and independent-gate FinFETs have been demonstrated\textsuperscript{2-4}.

The amount of embedded SRAM in modern microprocessors and systems-on-chips (SoCs) increases to meet the performance requirements in each new technology generation\textsuperscript{5}. Lower voltages and smaller devices cause a significant degradation in SRAM cell data stability with the scaling of CMOS technology. Maintaining the data stability of SRAM cells is expected to become increasingly challenging as the device dimensions are scaled to the sub-45 nm regime. In addition to the data stability issues, SRAM circuits are also important sources of leakage due to the enormous number of transistors in the memory caches. The development of a robust SRAM cell that can provide enhanced memory integration density and lower leakage power consumption with the emerging FinFET technologies is highly desirable.
In Ref. [15] a functional tied-gate FinFET SRAM circuit is experimentally demonstrated. The sizes of the pull-down transistors are increased for data stability at the expense of higher leakage power and cell area. In Ref. [17] asymmetric independent-gate FinFET SRAM cells are presented. The back gate of the pull-down and access transistors of the entire row are modulated with a specialized wordline driver. Multiple supply voltages are employed to reduce leakage and enhance stability. However, the circuit complexity increases and the supply voltages variations become more significant when multiple supply voltages are employed. In Refs. [14] and [16] a minimum sized independent-gate FinFET SRAM cell is presented. The back gates of the access transistors are connected to the corresponding storage nodes for dynamically enhancing both read and write margins. With this SRAM cell, however, the standby leakage power and the bitline leakage are increased due to the lower threshold voltage of the access transistors with a turned on back gate. In Ref. [14], another SRAM cell is presented that is based on multiple fin orientations for achieving higher on current with the pull-down transistors without increasing the sizes of these transistors. Having multiple fin orientations is, however, challenging from a manufacturing perspective with potentially higher susceptibility to process variations.

A new 6T independent-gate FinFET SRAM circuit with PMOS access transistors is proposed in this paper for simultaneously reducing the power consumption and the circuit area while enhancing the data stability of static memory circuits. All of the six transistors of an independent-gate FinFET SRAM cell are sized minimum without sacrificing functionality and data stability with the new technique. The voltage disturbances at the data storage nodes are reduced and the pull-up strengths of the cross-coupled inverters are enhanced during a read operation by employing PMOS access transistors. The data stability is thereby enhanced without the need for increasing the sizes of the transistors in the cross-coupled inverters. One gate of each pull-up FinFET is permanently disabled for achieving write ability with the proposed technique. The read static noise margin is enhanced by up to 62% with the new SRAM cell while reducing the leakage power by up to 22% as compared to a standard tied-gate FinFET SRAM cell with the same size transistors. Furthermore, the leakage power, the write power, and the layout area of the proposed SRAM cell are reduced by up to 62%, 16.5%, and 25.53% respectively, as compared to a standard FinFET SRAM cell sized for similar data stability in a 32 nm FinFET technology.

The paper is organized as follows. The FinFET technology is described in Section 2. The standard FinFET SRAM circuits and the new independent-gate FinFET SRAM circuit with P-type data access transistors are presented in Section 3. Data stability, power, delay, and area characteristics of the tied-gate and the independent-gate FinFET SRAM circuits are compared in Section 4. Finally, conclusions are offered in Section 5.

2. FinFET TECHNOLOGY

In this section the device architectures for tied-gate and independent-gate FinFETs are presented. N-type and P-type FinFETs with a 32 nm gate length are designed and characterized using Taurus-Medici, a physics-based device simulator. The effect of different gate bias conditions on the $I-V$ characteristics of independent-gate FinFETs is
Table I. Device technology parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Magnitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate length ($L$)</td>
<td>32 nm</td>
</tr>
<tr>
<td>Effective channel length ($L_{ee}$)</td>
<td>25.6 nm</td>
</tr>
<tr>
<td>Fin thickness ($t_{si}$)</td>
<td>8 nm</td>
</tr>
<tr>
<td>Fin height ($H_{fin}$)</td>
<td>32 nm</td>
</tr>
<tr>
<td>Oxide thickness ($t_{ox}$)</td>
<td>1.6 nm</td>
</tr>
<tr>
<td>Channel doping</td>
<td>$10^{15}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Source/drain doping</td>
<td>$2\times10^{20}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Gates work function (N-type FinFET)</td>
<td>4.5 eV</td>
</tr>
<tr>
<td>Gates work function (P-type FinFET)</td>
<td>4.9 eV</td>
</tr>
<tr>
<td>Medici physical models</td>
<td>AUGER, CONMOB SRFMOB, FLDMOB, and DT.CUR</td>
</tr>
</tbody>
</table>

The width of a FinFET is quantized due to the vertical gate structure. The fin height determines the minimum transistor width. Since the fin height is fixed in a FinFET technology, multiple parallel fins are utilized to increase the width of a FinFET, as shown in Figure 2. The two vertical gates of a FinFET can be separated by an oxide on top of the silicon fin, thereby forming an independent-gate FinFET as shown in Figure 1(b). An independent-gate FinFET provides two different active modes of operation with significantly different current characteristics determined by the bias conditions of the two independent gates as shown in Figure 3.

In the dual-gate-mode, the two gates are biased with the same signal to control the formation of a conducting channel in an independent-gate FinFET. Alternatively, in the single-gate-mode, one gate is biased with the input signal to induce channel inversion while the other gate is disabled (disabled gate: biased with $V_{GND}$ in an N-type FinFET and with $V_{DD}$ in a P-type FinFET). The two gates are strongly coupled in the dual-gate-mode, thereby lowering the threshold voltage ($|V_{th}|$) as compared to the single-gate-mode. The maximum drain current produced in the dual-gate-mode is therefore 2.6 (2.9) times higher as compared to the single-gate-mode for an N-type (P-type) FinFET in a 32 nm FinFET technology, as shown in Figure 3. Furthermore, the switched gate capacitance of a FinFET is halved in the single-gate-mode due to the disabled back gate. The unique $V_{th}$ modulation aspect of independent-gate FinFETs through selective gate bias is exploited in this paper to enhance the SRAM data stability and the integration density while lowering the static and dynamic power consumption with minimum sized transistors.

3. FinFET SRAM CELLS

The design considerations for the reliable operation of the 6T FinFET SRAM circuits are provided in this section. The tied-gate FinFET SRAM cells are discussed in Section 3.1. A previously published independent-gate FinFET SRAM circuit is described in Section 3.2. The new independent-gate FinFET SRAM circuit with PMOS access transistors is presented in Section 3.3.

3.1. Standard Tied-Gate FinFET SRAM Cells

The data stability of a memory circuit is most vulnerable to external noise during a read operation due to the intrinsic
disturbance produced by the direct data-read-access mechanism of the standard 6T SRAM cells. In order to maintain the read stability, the pull-down transistors must be stronger as compared to the bitline access transistors. Alternatively, for write ability, the bitline access transistors must be stronger as compared to the pull-up transistors.

Three tied-gate FinFET SRAM cells (SRAM-TG1, SRAM-TG2, and SRAM-TG3) with different sizes are considered in this paper, as shown in Figure 4. All of the six transistors in SRAM-TG1 are sized minimum (one fin), as shown in Figure 4(a). A minimum sized SRAM cell is highly desirable for maximizing the memory integration density. The noise immunity of SRAM-TG1 is, however, weak. For sufficient noise immunity and read stability the pull-down transistors of the inverters in a tied-gate FinFET SRAM cell should have at least two fins, as illustrated in Figures 4(b and c). The standard approach of transistor sizing to enhance the cell stability unfortunately also causes significantly higher leakage power consumption and larger cell area. The power and area overheads of the transistor sizing based data stabilization techniques are high particularly in a FinFET technology due to the quantized sizing of the transistors.

3.2. Previously Published Independent-Gate FinFET SRAM Cell

A previously published independent-gate FinFET SRAM cell (SRAM-IG1) is described in this section. All of the transistors in the SRAM-IG1 have single fin (minimum width) as shown in Figure 5. The idle mode leakage power consumption is reduced with SRAM-IG1 while enhancing the data stability as compared to the tied-gate FinFET SRAM circuits.

With SRAM-IG1, the pull-down transistors in the cross-coupled inverters are tied-gate FinFETs. Alternatively, the pull-up transistors in the cross-coupled inverters and the bitline access transistors are independent-gate FinFETs operating in the single-gate-mode. The access transistors act as weak high-\(V_t\) devices. The disturbance caused by the direct-data-access mechanism during read operations is thereby suppressed without the need for increasing the sizes of the pull-down transistors within the cross-coupled inverters. The data stability is therefore enhanced as compared to a tied-gate FinFET SRAM cell with the same size transistors. A minimum sized NMOS access transistor operating in the single-gate mode is significantly stronger as compared to a minimum sized PMOS pull-up transistor operating in the single gate mode, as listed in Table II. Write ability is therefore achieved by permanently operating the pull-up transistors in the single-gate-mode with SRAM-IG1.
The new independent-gate FinFET SRAM cell with P-Type Data Access Transistors

The new independent-gate FinFET SRAM cell with P-channel access transistors (SRAM-IG2) is presented in this section. All of the transistors in the SRAM-IG2 have single fin (minimum width) as shown in Figure 6. The leakage power consumption is reduced with SRAM-IG2 while enhancing the data stability as compared to both SRAM-TG1 and SRAM-TG1 with same size transistors. Furthermore, with SRAM-IG2, the leakage power is reduced and the integration density is enhanced while providing similar data stability as compared to SRAM-TG2 and SRAM-TG3.

With SRAM-IG2 the pull-down transistors in the cross-coupled inverters and the bitline access transistors are tied-gate FinFETs. Alternatively, the pull-up transistors within the cross-coupled inverters are independent-gate FinFETs operating in the single-gate-mode. The bitline access transistors are weak P-Type FinFETs as shown in Figure 6. The disturbance at the data storage nodes is therefore suppressed during a read operation thereby enhancing the data stability of SRAM-IG2. The bitline access transistors operating in the dual-gate-mode are stronger as compared to the pull-up transistors operating in the single-gate-mode (2.9 times higher on current in this 32 nm FinFET technology). The write-ability is thereby achieved with a high write margin with the proposed circuit.

The operation of SRAM-IG2 is as follows. The wordline WL is maintained at \( V_{DD} \) in an un-accessed SRAM cell. The bitline access transistors are turned off. The data in the SRAM cell is maintained by the cross-coupled inverters. The bitlines are periodically pre-charged to \( V_{DD} \).

WL transitions to \( V_{GND} \) to initiate a read operation. The access transistors P3 and P4 are turned on. Provided that Node1 stores “0”, BL is discharged through P3 and N1. Alternatively, provided that Node2 stores “0”, BLB is discharged through P4 and N2. The P-type FinFETs P3 and P4 are weaker with significantly higher resistance as compared to the N-type FinFETs N1 and N2. The intrinsic data disturbance that occurs due to the direct-data-read-access mechanism of the 6T SRAM cell topology is therefore significantly suppressed with SRAM-IG2. The P-type access transistors also enhance the pull-up strength on the side that stores a “1”. The read stability is thereby enhanced with the proposed SRAM circuit (SRAM-IG2) as compared to both the standard minimum sized tied-gate FinFET SRAM circuit and the previously published independent-gate FinFET SRAM circuit (SRAM-IG1).

The bitlines are periodically pre-charged to \( V_{DD} \). Prior to a write operation one of the bitlines is selectively discharged to \( V_{GND} \) depending on the data to be written to the SRAM cell. In order to write a “0” to Node1, the bitline (BL) is selectively discharged. Alternatively, for writing a “0” to Node2, the bitline-bar (BLB) is discharged. WL transitions to \( V_{GND} \) to initiate the write operation. The bitline access transistors are turned on. A “0” is forced onto the data storage node that is connected to the discharged bitline. The two access transistors P3 and P4 act as low-\(|V_{th}|\) devices operating in the dual-gate-mode. Alternatively, the pull-up transistors of the cross-coupled inverters (P1 and P2) act as weaker high-\(|V_{th}|\) devices operating in the single-gate-mode. Write ability is thereby achieved with a high write margin with the proposed SRAM cell. Note that the P-type access transistor that is connected to the discharged bitline can only discharge the data storage node to \( V_{DD} \). The transition to 0 V is completed by the positive feedback provided by the cross-coupled inverters with the assistance of the P-type access transistor that is connected to the charged bitline. To write a “0” onto Node1 BL is discharged to 0 V and BLB is charged to \( V_{DD} \) as shown in Figure 7. The bitline access transistors

**Table II.** DC characteristics of FinFETs (\( T = 70 ^\circ C \)).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Dual-gate mode</th>
<th>Single-gate mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{on} ) (nA/\mu m)</td>
<td>255</td>
<td>255</td>
</tr>
<tr>
<td>( I_{on} ) (mA/\mu m)</td>
<td>1.76</td>
<td>0.68</td>
</tr>
<tr>
<td>( V_{th} ) (V)</td>
<td>0.25</td>
<td>0.39</td>
</tr>
</tbody>
</table>

![Fig. 6.](image_url)

**Fig. 6.** The new independent-gate FinFET SRAM cell (SRAM-IG2) with P-type tied-gate data access transistors.

![Fig. 7.](image_url)

**Fig. 7.** Waveforms of the storage nodes of SRAM-IG2 during a write operation.
(P3 and P4) are turned on. Node1 is discharged to about $|V_{gS}|$ before P3 is turned off ($|V_{gS}|$ is about 0.3 V). When Node1 is at $|V_{gS}|$, P2 and P4 are both strongly turned on providing higher drain current as compared to N2. Node2 is charged all the way up to $V_{DD}$. Node1 is turned on. Node1 is thereby discharged all the way down to 0 V with the assistance of N1 after P3 is cut-off.

4. SIMULATION RESULTS

The read stability, the leakage power, the cell area, the active mode power, and the access delays of the three tied-gate FinFET SRAM cells (SRAM-TG1, SRAM-TG2, and SRAM-TG3) and the two independent-gate FinFET SRAM cells (SRAM-IG1 and SRAM-IG2) are compared in this section. The transistor sizing of the SRAM cells are as shown in Figures 4–6. The SRAM circuits are simulated at the nominal design corner and under process parameter variations using mixed-mode simulations with Taurus-Medici. The SRAM cells are characterized for different supply voltages.

4.1. Read Stability

Static noise margin (SNM) is the metric used in this paper to characterize the read stability of the SRAM cells. The SNM is the minimum DC noise voltage necessary to flip the state of an SRAM cell. The data stability of a 6T SRAM circuit is most vulnerable to external noise during a read operation due to the intrinsic disturbance produced by the direct data-read-access mechanism. It is assumed in this section, without loss of generality, that Node1 and Node2 store a “1” and a “0”, respectively. The read SNMs of the five SRAM cells are shown in Figure 8 with different supply voltages.

During a read operation with a 6T SRAM cell, the bitline access transistors are turned on after the bitlines are pre-charged to $V_{DD}$. The voltage of Node2 is raised due to the voltage division between the access and the pull-down transistors. The increased voltage of Node2 can also potentially result in a voltage drop at Node1 if the pull-up strength of the corresponding inverter is weak. The voltage disturbance at Node2 can be significantly suppressed either by employing stronger pull-down transistors (N1 and N2) with lower resistance as in SRAM-TG2 and SRAM-TG3 or by employing weaker independent-gate bitline access transistors with higher resistance operating in the single-gate-mode as in SRAM-IG1. The enhancement in data stability by transistor sizing in SRAM-TG2 and SRAM-TG3, however, comes with a significant increase in leakage power and area. Alternatively, with SRAM-IG1, the weaker bitline access transistors necessitate the utilization of even weaker pull-up transistors for achieving writeability. The weaker pull-up transistors with SRAM-IG1 degrade the data stability at the node that stores a “1”.

With the proposed SRAM circuit technique, the bitline access transistors are P-type tied-gate FinFETs. The tied-gate access transistors are intrinsically weaker with higher channel resistance as compared to the tied-gate N-type pull-down transistors. The disturbance at Node2 is therefore significantly suppressed during a read operation. Furthermore, with SRAM-IG2, the P-type access transistor P3 enhances the pull-up strength at Node1 during a read operation since P3 is in parallel with P1 (notice the shift in the DC transfer characteristics between the hold mode and the read mode in Fig. 9). Alternatively, with SRAM-TG1 and SRAM-IG1, the NMOS access transistor N3 does not play a significant role to strengthen the data storage at Node1. N3 is maintained cut-off until Node1 voltage is reduced significantly by a threshold voltage drop below $V_{DD}$ due to noise in SRAM-TG1 and SRAM-IG1. The read SNM of SRAM-IG2 is enhanced by 59.7%, 60%, and 62.3% as compared to SRAM-TG1 for $V_{DD} = 0.6$ V, 0.8 V, and 1 V, respectively. The read SNM of SRAM-IG2 is also enhanced by 10%, 11% , and 15% as compared to SRAM-IG1 for $V_{DD} = 0.6$ V, 0.8 V, and 1 V, respectively. The read

![Fig. 8. The read SNMs of the FinFET SRAM cells. $T = 70^\circ$C.](image)

![Fig. 9. Butterfly curves of SRAM-IG1 and SRAM-IG2 during the hold mode and for a read operation. $V_{DD} = 0.8$ V. $T = 70^\circ$C.](image)
SNMs of SRAM-IG2, SRAM-TG2, and SRAM-TG3 are similar.

4.2. Leakage Power Consumption

The leakage power consumption of the SRAM cells at 70 °C is shown in Figure 10 for different supply voltages. The leakage power of an SRAM cell is determined by the total effective transistor width that produces the leakage current. In SRAM-TG1, SRAM-IG1, and SRAM-IG2, all the transistors are sized minimum. Furthermore, with SRAM-IG2, the leakage current of the PMOS access transistors is lower as compared to the NMOS access transistors employed with the other SRAM cells. Note that a minimum sized P-channel FinFET produces significantly smaller sub-threshold and gate-oxide leakage currents as compared to a minimum sized N-channel FinFET as listed in Table II. SRAM-IG2 therefore consumes the lowest leakage power among the memory circuits considered in this paper. SRAM-IG2 consumes 21.3%, 21.4%, and 21.7% lower leakage power as compared to both SRAM-TG1 and SRAM-IG1 at VDD = 0.6 V, 0.8 V, and 1 V, respectively. Transistor sizing for enhanced data stability comes at a significant cost of additional leakage power with SRAM-TG2 and SRAM-TG3, as illustrated in Figure 10. The leakage power consumed by SRAM-IG2 is 61.8%, 61.5%, and 61.4% lower as compared to SRAM-TG3 for VDD = 0.6 V, 0.8 V, and 1 V, respectively. Furthermore, by utilizing minimum sized P-type access transistors, the bitline leakage current is reduced by 62%, 61.2%, and 61% with SRAM-IG2 as compared to the other SRAM circuits at VDD = 0.6 V, 0.8 V, and 1 V, respectively, as shown in Figure 11.

4.3. SRAM Cell Area

The thin-cell layouts of the SRAM cells are shown in Figure 12. The layout rules are listed in Table III. The fin pitch is assumed to be 6 times the fin thickness in the layouts. SRAM-TG1 and SRAM-IG2 have the smallest area since all six transistors are sized minimum with only one fin. SRAM-IG1 occupies a larger cell area (23% larger as compared to SRAM-IG2) due to the extra contacts. SRAM-TG2 and SRAM-TG3 occupy a larger area as compared to SRAM-IG2 due to the larger pull-down transistors. The areas of SRAM-TG2 and SRAM-TG3 are 17% and 34% larger as compared to SRAM-IG2, respectively. Furthermore, only one metal layer is used within the SRAM-IG2 cell unlike SRAM-IG1 that requires the utilization of two metal layers, as shown in Figure 12. Note that the extra contacts with SRAM-IG2 do not increase the cell area since these contacts are shared between neighboring cells in a memory array.

4.4. Active Mode Power and Access Speed

The junction and gate-oxide capacitances of the access transistors are extracted for each SRAM cell. The lengths of the bitlines and the wordlines are estimated based on the cell layout dimensions. II-type RC networks that represent the bitline and the wordline parasitics of a 256 bit × 128 bit memory array are attached to each SRAM circuit. The normalized active mode power consumptions and delays of the five FinFET SRAM circuits are shown in Figure 13 for different supply voltages (VDD = 0.6 V, 0.8 V, and 1 V). The read delay is the time period from the 50% point of the WL low-to-high (high-to-low in case of SRAM-IG2) transition until a 200 mV voltage difference is developed between the bitlines. The write delay is the time period from the 50% point of the WL low-to-high (high-to-low in case of SRAM-IG2) transition until the storage node is discharged to VDD/2 (from an initial voltage of VDD). The read and write power consumptions include the power consumed to pre-charge the bitlines, the wordline driver power consumption, and the SRAM cell power consumption.

SRAM-IG1 consumes the lowest read and write power and has the shortest write delay due to the smaller wordline and internal node parasitic capacitances as compared to the other SRAM cells. Alternatively, SRAM-IG1 has the longest read delay due to the weaker access transistors. The read delay of SRAM-IG1 is 109%, 76%, and 59% longer as compared to SRAM-TG1 for VDD = 0.6 V, 0.8 V, and 1 V, respectively.
The write power of SRAM-IG2 is lower than SRAM-TG2 and SRAM-TG3 due to the smaller wordline parasitics and the smaller internal node capacitances. The write power of SRAM-IG2 is also lower than SRAM-TG1 due to the smaller internal node capacitances. The write power of SRAM-IG2 is reduced by 16.52%, 9%, and 12% as compared to SRAM-TG3 for \( V_{DD} = 0.6 \) V, 0.8 V, and 1 V, respectively. The read delay of SRAM-IG2 is 85%, 43%, and 31% longer as compared to SRAM-TG1 for \( V_{DD} = 0.6 \) V, 0.8 V, and 1 V, respectively. The read delay penalty with SRAM-IG2 is significantly lower as compared to SRAM-IG1 since a single fin PMOS access transistor operating in the dual-gate-mode produces higher on current as compared to a single fin NMOS transistors operating in the single-gate-mode as listed in Table II.

Writing to an SRAM cell is achieved by discharging one of the bitlines to ground and maintaining the other bitline at \( V_{DD} \). Successful writing to an SRAM cell can also be achieved with a voltage higher than 0 V on the discharged bitline (incomplete/partially discharged bitline). The write margin is the maximum voltage of the partially discharged

**Table III.** Layout rules.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate length</td>
<td>2( \lambda )</td>
</tr>
<tr>
<td>Fin thickness</td>
<td>( \lambda/2 )</td>
</tr>
<tr>
<td>Fin pitch ((6 \times \text{fin thickness}))</td>
<td>3( \lambda )</td>
</tr>
<tr>
<td>Contact hole</td>
<td>2( \lambda \times 2\lambda )</td>
</tr>
<tr>
<td>Contact size</td>
<td>4( \lambda \times 4\lambda )</td>
</tr>
<tr>
<td>Metal1 and metal2 width</td>
<td>4( \lambda )</td>
</tr>
<tr>
<td>Contact–contact separation</td>
<td>2( \lambda )</td>
</tr>
<tr>
<td>Active to active separation (\text{same type})</td>
<td>3( \lambda )</td>
</tr>
<tr>
<td>Active to active separation (\text{opposite type})</td>
<td>4( \lambda )</td>
</tr>
<tr>
<td>Poly to active separation</td>
<td>2( \lambda )</td>
</tr>
<tr>
<td>Poly to poly separation</td>
<td>3( \lambda )</td>
</tr>
<tr>
<td>Metal to metal separation</td>
<td>2( \lambda )</td>
</tr>
</tbody>
</table>
Fig. 13. The active mode power consumption and propagation delays of the SRAM circuits. For each SRAM circuit, the power and delay are normalized with respect to SRAM-TG1. $T = 70 \, ^\circ\text{C}$. (a) $V_{\text{dd}} = 0.6 \, \text{V}$. (b) $V_{\text{dd}} = 0.8 \, \text{V}$. (c) $V_{\text{dd}} = 1 \, \text{V}$.

bitline that achieves a successful transfer of a “0” into the 6T SRAM cell.\textsuperscript{12,14} The write margin is measured differently in this section as compared to Refs. [12] and [14] since the two bitlines assist in the writing of the proposed SRAM cell. The write margin is measured in this section as the maximum voltage amplitude of a DC noise signal that is applied to the two bitlines with equal amplitudes and opposite polarity for which a successful writing is achieved. The polarity of the DC noise signal that is applied to the discharged (charged) bitline is positive (negative). The content of an SRAM cell with a higher write margin is easier to be modified. The write margins for the SRAM circuits are listed in Table IV.

The write margin of the tied-gate FinFET SRAM cells is reduced when the size of the pull-down transistors is increased due to the reduced switching threshold voltage of the cross-coupled inverters and due to the increased internal node capacitances. The write margin of the proposed SRAM-IG2 is enhanced by up to 30% and 76% as compared to SRAM-TG2 and SRAM-TG3, respectively, due to the reduced internal node parasitic capacitances. Alternatively, the write margin of SRAM-IG2 is up to 98% higher as compared to SRAM-IG1 due to the stronger access transistors (refer to Table II).

From an application point of view, SRAM-IG2 is the most attractive choice at the higher levels of memory banks for which the enhanced integration density and the lower leakage power consumption are the most important design criteria. Alternatively, for a speed-critical first level cache with a smaller amount of memory, the SRAM-TG2 can be attractive despite the larger cell area, due to the higher read speed with reasonable write speed and data stability. SRAM-TG1 is not a practical choice due to the unacceptably small read static noise margin.

4.5. Process Variations

The effect of process variations on the tied-gate and the independent-gate FinFET SRAM cells is evaluated in this section. 1500 Monte-Carlo simulations are run with Taurus-Medici using a PERL script. The channel length, the fin height, the fin thickness, and the gate oxide thickness are assumed to have independent Gaussian distributions. The parameters of each transistor are varied independently except for the multi-fin FETs. For the multi-fin FETs, full correlation between the fins is assumed. The channel length and the fin thickness have $3\sigma$ variations of 20%. The fin height has a $3\sigma$ variation of 10%. The oxide thickness has a $3\sigma$ variation of 5%. The statistical distributions of the leakage power are shown in Figures 14 and 15 for $T = 27 \, ^\circ\text{C}$ and $T = 70 \, ^\circ\text{C}$, respectively. The statistical distributions of the SNM of the SRAM cells are shown in Figures 16 and 17 for $T = 27 \, ^\circ\text{C}$ and $T = 70 \, ^\circ\text{C}$, respectively.

With the proposed independent-gate SRAM cell SRAM-IG2, the mean and the standard deviation (SD) of the leakage power are reduced by 64.5% and 66.4%, respectively, as compared to SRAM-TG3 at room temperature as shown in Figure 13. The mean and the standard deviation (SD) of the leakage power are reduced by 61% and 65%, respectively, with SRAM-IG2 as compared to SRAM-TG3 at $T = 70 \, ^\circ\text{C}$ as shown in Figure 15. Furthermore, with

Table IV. The write margins of the SRAM cells ($T = 70 \, ^\circ\text{C}$).

<table>
<thead>
<tr>
<th>SRAM cell</th>
<th>$V_{\text{dd}} = 0.6 , \text{V}$</th>
<th>$V_{\text{dd}} = 0.8 , \text{V}$</th>
<th>$V_{\text{dd}} = 1 , \text{V}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM-TG1</td>
<td>227</td>
<td>306</td>
<td>395</td>
</tr>
<tr>
<td>SRAM-TG2</td>
<td>162</td>
<td>202</td>
<td>242</td>
</tr>
<tr>
<td>SRAM-TG3</td>
<td>127</td>
<td>153</td>
<td>180</td>
</tr>
<tr>
<td>SRAM-IG1</td>
<td>96</td>
<td>127</td>
<td>160</td>
</tr>
<tr>
<td>SRAM-IG2</td>
<td>183</td>
<td>250</td>
<td>316</td>
</tr>
</tbody>
</table>
Robust FinFET Memory Circuits with P-Type Data Access Transistors

Tawfik and Kursun

SRAM-TG1/ SRAM-IG1
Mean = 3 nW, SD = 0.9 nW
SRAM-TG2
Mean = 4.8 nW, SD = 1.6 nW
SRAM-TG3
Mean = 6.5 nW, SD = 2.3 nW
SRAM-IG2
Mean = 2.3 nW, SD = 0.8 nW

Fig. 14. Statistical leakage power distributions of the FinFET SRAM cells. $V_{DD}=0.8$ V. $T=27^\circ$C. SD: standard deviation.

SRAM-IG2 the mean SNM is enhanced by 55% and 60% as compared to SRAM-TG1 for $T=27^\circ$C (shown in Fig. 16) and $T=70^\circ$C (shown in Fig. 17), respectively.

The write margin is evaluated under process parameter, supply voltage, and temperature variations. The FinFET on current distribution is generated with 1000 samples assuming independent Gaussian distributions for the channel length (20% $3\sigma$ variation), the fin thickness (20% $3\sigma$ variation), the oxide thickness (5% $3\sigma$ variation), and the fin height (10% $3\sigma$ variation). The parameters of the strong and the weak devices are identified from the FinFET on current distributions. The on current of the weak device is lower than the mean on current by one sigma. Alternatively, the on current of the strong device is higher than the mean on current by one sigma, as shown in Figure 18.

The worst case process corner for write margin is the process corner characterized by the weak bitline access transistors and the strong pull-up transistors. The write margins of the SRAM cells at the worst case process corner are listed in Table V for different temperatures and supply voltages. As shown in Table V, SRAM-IG2 has higher write margin as compared to SRAM-TG2, SRAM-TG3, and SRAM-IG1. The write margin of SRAM-IG2 is enhanced by up to two-times ($\sim 2X$) as compared to SRAM-IG1 depending on the supply voltage and the temperature.

SRAM-TG1
Mean = 135 mV
SRAM-IG2
Mean = 208 mV

Fig. 16. Statistical SNM distributions of the FinFET SRAM cells. $V_{DD}=0.8$ V. $T=27^\circ$C.

SRAM-TG1
Mean = 124 mV
SRAM-IG2
Mean = 198.4 mV

60% higher

Fig. 17. Statistical SNM distributions of the FinFET SRAM cells. $V_{DD}=0.8$ V. $T=70^\circ$C.

Fig. 18. 1000 samples Monte-Carlo statistical distributions of the on-current of the single-fin FinFETs operating in the dual-gate mode. $V_{DD}=0.8$ V. $T=70^\circ$C.

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5. CONCLUSIONS

A new independent-gate FinFET SRAM cell is proposed in this paper for simultaneously enhancing the read data stability and the memory integration density while reducing the standby power consumption. All of the six transistors of the proposed SRAM cell are sized minimum. The voltage disturbance at the data storage nodes during a read operation is reduced by employing P-type bitline access transistors. The pull-up FinFETs in the cross-coupled inverters are permanently operated in the single-gate-mode with the proposed SRAM cell, thereby achieving write-ability with minimum sized transistors. The read SNM is enhanced by up to 62% with the proposed independent-gate FinFET SRAM cell while reducing the leakage power by up to 22% as compared to a tied-gate FinFET SRAM cell with the same size transistors. Alternatively, as compared to a 6 T tied-gate FinFET SRAM cell that is sized for comparable read static noise margin, the leakage power, the write power, and the cell area are reduced by up to 62%, 16.5%, and 25.53%, respectively.

References


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