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Temperature-adaptive voltage tuning for enhanced energy efficiency in ultra-low-voltage circuits

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Abstract

Circuits optimized for minimum energy consumption operate typically in the subthreshold regime with ultra-low power-supply voltages. Speed of a subthreshold logic circuit is enhanced with an increase in the die temperature. The excessive timing slack observed in the clock period of subthreshold logic circuits at elevated temperatures provides opportunities to lower the active-mode energy consumption. A temperature-adaptive dynamic-supply voltage-tuning technique is proposed in this paper to reduce the high-temperature energy consumption without degrading the clock frequency in ultra-low-voltage subthreshold logic circuits. Results indicate that the energy consumption can be lowered by up to 40% by dynamically scaling the supply voltage at elevated temperatures. An alternative technique based on temperature-adaptive reverse body bias to exponentially reduce the subthreshold leakage currents at elevated temperatures is also investigated. The active-mode energy consumption with two temperature-adaptive voltage-tuning techniques is compared. The impact of the process parameter and supply voltage variations on the proposed temperature-adaptive voltage scaling techniques is evaluated.

Keywords: Adaptive body bias; Dynamic voltage scaling; Reversed temperature dependence; Supply voltage tuning; Subthreshold logic; Temperature variations; Threshold voltage tuning

1. Introduction

There is a growing interest in ultra-low-power design methodologies due to the increasing market demand for extended battery lifetimes in portable devices and self-sustaining energy-scavenging battery-replacement-free systems [1]. Emerging applications with relatively low throughput requirements, such as distributed sensor networks, are typically aimed at lowering the energy consumption rather than achieving higher clock frequency. Scaling the supply voltage enhances the energy efficiency primarily by reducing the dynamic switching energy. The supply voltages that provide minimum energy consumption are typically observed in the subthreshold region, as reported in [1,3].

Integrated circuits with ultra-low-voltage power supplies are highly sensitive to process and temperature variations [4]. As the supply voltage is scaled to minimize the energy consumption, the supply voltage to threshold voltage ratio is reduced. The temperature-fluctuation-induced threshold voltage variations therefore determine the MOSFET drain current variations when the temperature fluctuates in circuits with extremely low power-supply voltages [2]. Contrary to the standard-higher-voltage circuits designed for high speed, low-voltage circuits optimized for minimum energy operate faster when the die temperature increases.

Variations in the die temperature are caused by the imbalanced switching activity within a die and/or the fluctuations in the environmental temperature. In circuits optimized for minimum energy consumption, on-chip temperature gradients induced by imbalanced switching activity are typically small. Die temperature fluctuations due to variations in the ambient temperature, however, can cause significant fluctuations in the speed and power characteristics of ultra-low-voltage circuits. For example, the integrated circuits employed in robotic explorations experience ambient temperatures that vary from −180 to

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486 °C [13]. Similarly, ultra-low-power sensor-net modules in security and healthcare applications are designed for functionality at a temperature range of −25 to –125 °C [15].

Dynamic supply voltage scaling technique is primarily used for reducing the active-mode power consumption of an integrated circuit by exploiting the variations in the computational workload [5–8]. Alternatively, the adaptive body-bias technique reduces both the active- and the standby-mode power consumption by dynamically adjusting the device threshold voltages depending on the variations of the workload and the circuit activity [5,8,9]. In this paper, a new temperature-adaptive dynamic supply voltage-tuning technique is proposed for reducing the active-mode energy consumption by exploiting the excessive timing slack produced in the clock period of ultra-low-voltage CMOS circuits at elevated temperatures. The high-temperature energy efficiency is enhanced while maintaining a constant clock frequency by dynamically scaling the supply voltage of a subthreshold logic circuit. The supply voltages that lower the energy consumption without degrading the circuit speed at increased temperatures are identified for circuits in the TSMC 180 nm CMOS technology [16]. An alternative technique based on temperature-adaptive threshold voltage tuning through reverse body bias is also investigated. The active-mode energy consumption characteristics of the two temperature-adaptive voltage-tuning techniques are compared. The effectiveness of the proposed temperature-adaptive supply voltage-tuning technique is also evaluated under process parameter and supply voltage variations.

The paper is organized as follows. The effects of temperature fluctuations on the device and circuit characteristics are examined in Section 2. A design methodology to identify the supply voltages providing minimum energy in the standard constant-V_{DD} and constant-frequency systems is presented in Section 3. The new temperature-adaptive supply and threshold voltage scaling techniques for dynamically reducing the energy consumed at high die temperatures are described in Section 4. The energy characteristics of the temperature-adaptive schemes and the impact of the process parameter and supply voltage variations on the proposed methodologies are evaluated in Section 5. Finally, some conclusions are provided in Section 6.

2. Device and circuit behavior under temperature fluctuations

The effects of temperature fluctuations on the device and circuit characteristics are reviewed in this section. An increase in the die temperature degrades the absolute values of threshold voltage, carrier mobility, and saturation velocity of MOSFETs [2,10,11,19]. The saturation velocity is typically a weak function of temperature [11]. Threshold voltage degradation with temperature tends to enhance the drain current because of the increase in gate overdrive $|V_{GS}-V_t|$. Alternatively, degradation in carrier mobility tends to lower the MOSFET drain current [2,12,19]. Effective variation of MOSFET drain current is determined by the variation of the dominant device parameter when the temperature fluctuates. Gate overdrive and carrier mobility variations due to temperature fluctuations at different supply voltages for devices in a 180 nm CMOS technology are listed in Table 1. Variation of the MOSFET drain current (I_{DS}) with the supply voltage and the temperature is shown in Fig. 1.

For devices operating at the nominal supply voltage ($V_{DD} = 1.8$ V), variations in gate overdrive are smaller as compared to carrier mobility fluctuations when the temperature is increased from 25 to 125 °C, as listed in Table 1. The MOSFET drain current is therefore reduced, following the degradation of carrier mobility at elevated temperatures, as shown in Fig. 1 [2,12]. The propagation delay of a circuit is dependent on the drain saturation current produced by active devices [5]. The reduction of the MOSFET drain current degrades the circuit speed when

Table 1
Gate overdrive and carrier mobility variations at different supply voltages

Supply voltage (V)	Temperature (°C)	Gate overdrive (V)		Carrier mobility ($\times 10^{-3}$ m^2/V s)	
		PMOS	NMOS	PMOS	NMOS
1.8	25	−1.34	1.33	5.46	28.86
	125	−1.41	1.39	4.47	17.93
	Variation (%)	5.37	4.95	−18.26	−37.87
1.1	25	−0.64	0.63	6.31	35.10
	125	−0.71	0.69	5.13	20.08
	Variation (%)	11.28	10.48	−18.69	−42.78
0.7	25	−0.24	0.23	6.98	37.78
	125	−0.31	0.29	5.70	20.95
	Variation (%)	30.39	29.01	−18.36	−44.54
0.5	25	−0.04	0.03	7.39	38.66
	125	−0.11	0.09	6.06	21.25
	Variation (%)	198.88	249.31	−17.98	−45.03

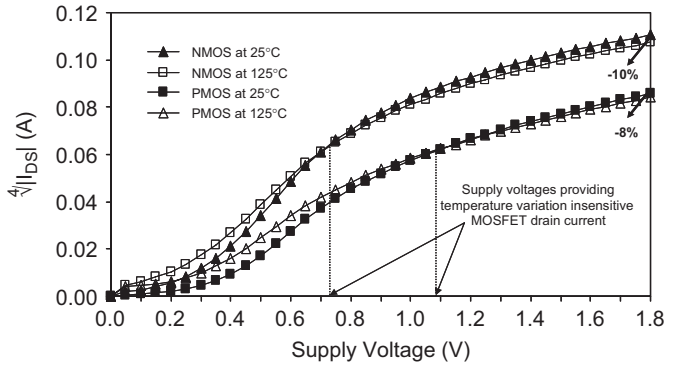

Fig. 1. Variation of MOSFET drain current (I_{DS}) with supply voltage (V_{DD}) and temperature in a 180 nm CMOS technology. $|V_{DS}| = |V_{GS}| = V_{DD}$.

the die temperature increases at the nominal supply voltage ($V_{DD} = 1.8$ V) [12,19].

The sensitivity of gate overdrive to temperature fluctuations is enhanced at scaled supply voltages, as listed in Table 1 [12]. For a particular lower supply voltage ($V_{DD} = 1.09$ V for PMOS and $V_{DD} = 0.72$ V for NMOS), the temperature-fluctuation-induced gate overdrive variation completely counterbalances the carrier mobility variation, thereby providing temperature-variation-insensitive constant MOSFET drain current, as shown in Fig. 1 [2,12]. Circuits operating with a specific supply voltage within this range ($0.72\text{ V} < V_{DD} < 1.09\text{ V}$) exhibit temperature-variation-insensitive propagation-delay characteristics [12]. Further scaling of the supply voltage reverses the temperature-dependent speed characteristics of CMOS circuits. The enhanced variations of the gate-overdrive voltage begin to determine the propagation-delay fluctuations with the temperature. Integrated circuits with ultra-low power-supply voltages therefore operate faster when the die temperature increases [12].

3. Supply-voltage optimization for minimizing energy consumption

The mobile products that rely on battery lifetime and the self-sustaining integrated systems with energy-scavenging capability require ultra-low-power integrated circuits. Power consumption of CMOS circuits can be lowered by employing several techniques as described in [5–9]. In this section, a design methodology for minimizing the energy consumption of CMOS circuits is described.

The two primary sources of power dissipation in CMOS circuits are the static power, which results from leakage currents of the MOSFETs, and the dynamic power, which results from the switching activity. The energy consumed per cycle is

$$\text{Energy}_{\text{Total}} \approx \text{Energy}_{\text{Switching}} + \text{Energy}_{\text{Leakage}}, \quad (1)$$

$$\text{Energy}_{\text{Switching}} \propto V_{DD}^2, \quad (2)$$

$$\text{Energy}_{\text{Leakage}} = I_{\text{Leakage}} V_{DD} T, \quad (3)$$

where $\text{Energy}_{\text{Total}}$, $\text{Energy}_{\text{Switching}}$, $\text{Energy}_{\text{Leakage}}$, I_{Leakage}, V_{DD}, and T are the total energy consumed per cycle, total dynamic switching energy per cycle, total leakage energy per cycle, total leakage current, supply voltage, and cycle time, respectively. The energy efficiency of an integrated circuit (IC) can be enhanced by scaling the power-supply voltage [2]. Supply-voltage scaling quadratically reduces the dynamic switching energy, as given by (2). Scaling the supply voltage, however, also increases the total leakage energy per cycle as given by (3), due to the increase in the clock period [1]. The total energy consumed by an IC, therefore, has a minimum as the supply voltage is scaled.

Standard ICs are designed to operate with a constant supply voltage (constant-V_{DD}) at a constant frequency (constant-f_s) under different environmental conditions. An algorithm that optimizes the supply voltage of a standard constant-V_{DD} (with no supply-voltage scaling capability) and constant-f_s (with no frequency scaling capability) IC for achieving minimum energy consumption is illustrated in Fig. 2, assuming a $T_1 \rightarrow T_2$ die temperature spectrum. $V_{DD\text{-nom}}$, $V_{DD\text{-min}}$, and V_{step} are the nominal supply voltage, the lowest applicable supply voltage below which malfunction occurs, and the voltage scaling resolution, respectively. $V_{DD\text{-nom}}$ is technology-dependent (1.8 V for a 180 nm CMOS technology) and V_{step} is assumed to be 10 mV in this paper. In the first iterative part of the algorithm, the supply voltage is scaled with a voltage resolution of V_{step}. The highest constant clock frequency that can be maintained within the entire temperature spectrum is identified for each supply voltage. In the second part of the algorithm, the energy consumed by the circuit is measured at various temperatures of interest for each pair of supply voltage and the corresponding highest achievable clock frequency. From the measured energy consumption, the constant supply voltage that achieves minimum energy at a specific temperature (within the temperature spectrum) is identified, assuming a standard constant-V_{DD} and constant-f_s circuit operation.

The methodology used in this paper to measure the maximum frequency (f_{max}) achievable with a circuit at a specific supply voltage and temperature is illustrated here using the input/output waveforms shown in Fig. 3. Circuits can be either inverting or non-inverting. The input and output waveforms of an inverting circuit are shown in Fig. 3. The integrated circuit is initially operated at a low frequency ($f \ll f_{max}$, where f_{max} needs to be determined). Time_1 is the time taken for the falling (rising) output signal to cross $0.1*V_{DD}$ ($0.9*V_{DD}$) after the rising input signal crosses $0.1*V_{DD}$ ($0.1*V_{DD}$) in an inverting (non-inverting) circuit. Similarly, Time_2 is the time taken for the rising (falling) output signal to cross $0.9*V_{DD}$ ($0.1*V_{DD}$) after the falling input signal crosses $0.9*V_{DD}$ ($0.9*V_{DD}$) in an inverting (non-inverting) circuit. A 20% margin is added to the maximum of Time_1 and Time_2 to provide timing slack against parameter variations and clock skew. The maximum frequency of a circuit at a specific supply voltage

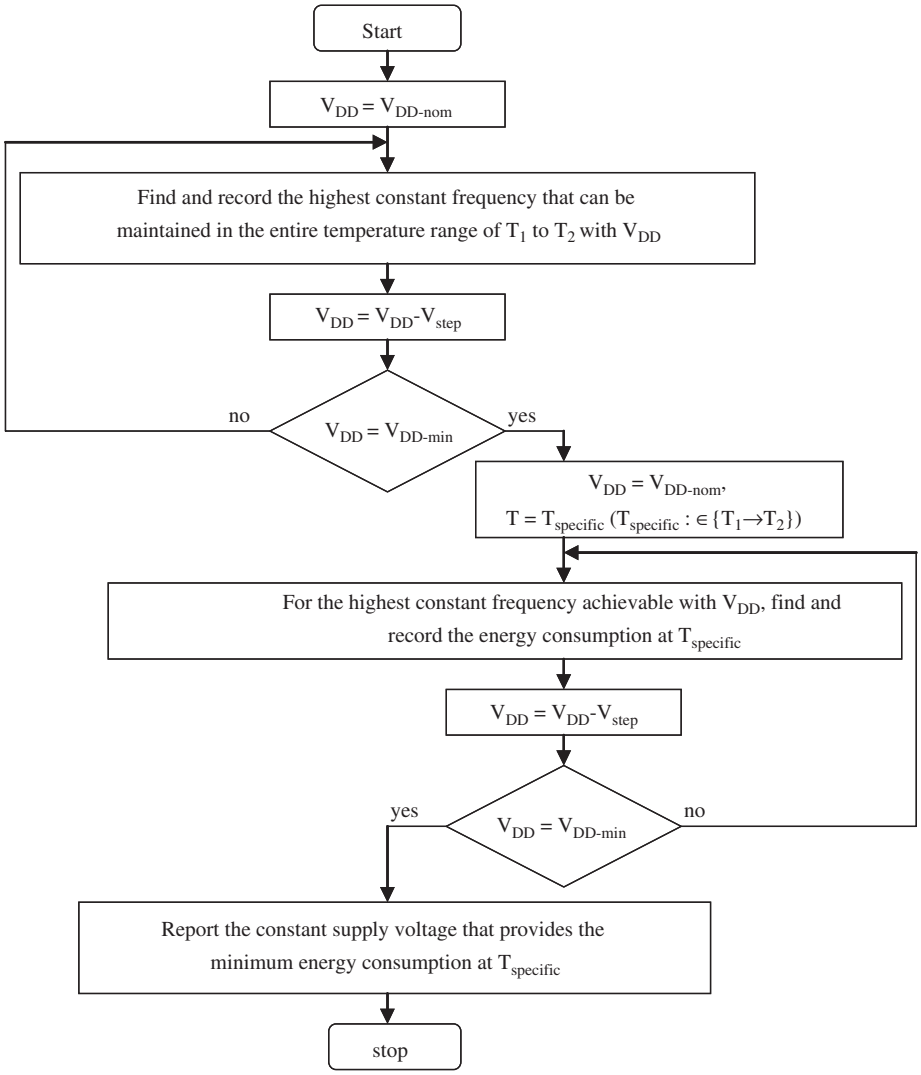

Fig. 2. Flow chart for identifying the supply voltage that achieves minimum energy consumption at a specific temperature ($T_{specific}$) for a standard constant-V_{DD} and constant-f_s IC.

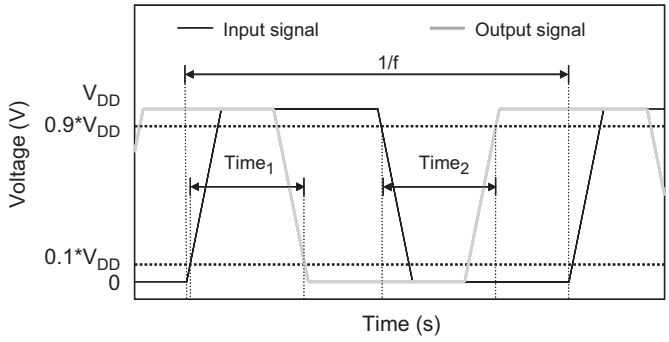

Fig. 3. The input and output waveforms of an inverting circuit.

and temperature is

$$f_{max} = \frac{1}{2*1.2*\max(Time_1, Time_2)}. \quad (4)$$

To find the highest achievable constant clock frequency at a particular supply voltage, the maximum achievable frequencies (f_{max}) at the extremes of the die temperature spectrum (T_1 and T_2) are measured using the above procedure. The smaller of the two frequencies is the highest constant frequency that can be maintained by the circuit within the entire temperature spectrum ($T_1 \rightarrow T_2$) at the particular supply voltage.

The results of the algorithm are listed in Table 2 for a 16-bit Brent–Kung adder in a 180 nm CMOS technology. The die temperature spectrum is assumed to be from 25 to 125 °C. The standard constant supply voltages for achieving minimum energy consumption at 25 and 125 °C are reported. As listed in Table 2, the temperature that determines the highest operating frequency is also dependent on the supply voltage of the circuit. At the higher supply voltages (such as the nominal-$V_{DD} = 1.8$ V), circuits operate slower when the die temperature increases. The maximum achievable (worst-case) frequency is therefore

Table 2
Supply voltages that achieve minimum energy in a constant-V_{DD} and constant-f_s Brent–Kung adder

V_{DD} (V)	Maximum frequency at 25 °C (MHz)	Maximum frequency at 125 °C (MHz)	Worst-case frequency (MHz)	Energy consumption at the worst-case frequency and 25 °C (pJ)	Energy consumption at the worst case frequency and 125 °C (pJ)
1.80	296.56	265.14	265.14	2.0000	2.0400
1.20	173.96	162.68	162.68	0.8370	0.8510
0.99	117.57	116.84	116.84	0.5531	0.5637
0.98	115.62	115.23	115.23	0.5464	0.5524
0.97[a]	110.78	111.99	110.78	0.5344	0.5354
0.49	3.91	11.00	3.91	0.1200	0.1500
0.48	3.26	9.94	3.26	0.1160	0.1490
0.47[b]	2.70	8.87	2.70	0.1110	0.1480[c]
0.46	2.37	7.90	2.37	0.1060	0.1500
0.45	1.94	6.86	1.94	0.1020	0.1520
0.28	0.052	0.620	0.052	0.0495	1.1200
0.27	0.041	0.530	0.041	0.0488	1.3600
0.26[d]	0.032	0.45	0.032	0.0480[e]	1.6600
0.25	0.025	0.39	0.025	0.0485	2.0200
0.24	0.020	0.33	0.020	0.0493	2.4600

Results are for a Brent–Kung adder in a 180 nm CMOS technology.
[a]Supply voltage below which the circuit exhibits reverse temperature dependence.
[b]$V_{DD\text{-}125}$.
[c]Minimum energy at 125 °C.
[d]$V_{DD\text{-}25}$.
[e]Minimum energy at 25 °C.

determined by plugging the low-to-high and high-to-low critical path propagation delays observed at the highest temperature into (4). Alternatively, as the supply voltage is scaled, the worst-case speed shifts to the lowest operating temperature, as listed in Table 2, due to the determination of the propagation-delay characteristics primarily by the gate overdrive variations of the MOSFETs below a specific V_{DD} (0.97 V for this Brent–Kung adder). The maximum achievable clock frequency for an entire temperature spectrum is therefore determined by the critical path delays observed at the lowest temperature for $V_{DD} \leqslant 0.97$ V. $V_{DD\text{-}25}$ and $V_{DD\text{-}125}$ are the constant supply voltages applied to a standard CMOS circuit (without any voltage-tuning capability) for achieving minimum energy consumption at 25 and 125 °C, respectively. The supply voltage that provides minimum energy consumption varies with the operating temperature. The energy consumption of the 16-bit Brent–Kung adder at different temperatures along with the supply voltage that minimizes the energy consumption at each temperature is shown in Fig. 4.

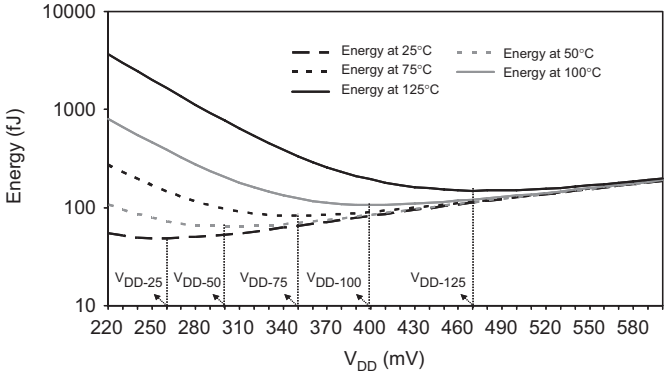

Fig. 4. Supply voltages that minimize the energy consumption of the 16-bit Brent-Kung adder at different temperatures. $V_{DD\text{-}25}$, $V_{DD\text{-}50}$, $V_{DD\text{-}75}$, $V_{DD\text{-}100}$, and $V_{DD\text{-}125}$ are the supply voltages providing minimum energy consumption at 25, 50, 75, 100, and 125 °C, respectively.

The supply voltage that provides minimum energy is determined by the relative significance of dynamic switching and leakage energy components [1]. The subthreshold leakage current produced by a MOSFET is [5]

$$\text{leak} = \frac{\mu W_{\text{eff}} C_{\text{OX}}}{L_{\text{eff}}} V_{\text{T}}^2 e^{(|V_{\text{GS}}|-|V_{\text{t}}|)/nV_{\text{T}}}(1 - e^{-|V_{\text{DS}}|/V_{\text{T}}}), \qquad (5)$$

where I_{leak}, μ, W_{eff}, C_{OX}, L_{eff}, V_{t}, V_{T}, V_{GS}, V_{DS}, and n are the subthreshold leakage current, carrier mobility, effective transistor width, oxide capacitance per unit area, effective channel length, threshold voltage, thermal voltage, gate-to-source voltage, drain-to-source voltage, and subthreshold swing coefficient, respectively.

Absolute value of the threshold voltage degrades as the temperature increases [10,11]. Degradation of the threshold voltage coupled with the enhancement of the thermal voltage exponentially increases the subthreshold leakage current at higher temperatures, as given by (5). The supply voltages that minimize the energy consumption are higher for circuits with relatively higher leakage currents [1]. Minimum energy at an elevated temperature is therefore observed at a higher supply voltage, as listed in Table 1 and as shown in Fig. 4. The algorithm is executed on multiple test circuits and the supply voltages that minimize the

Table 3
Supply voltages for achieving minimum energy in standard constant-V_{DD} and constant-f_s circuits

Circuits in a 180 nm CMOS technology	Supply voltages (V)	
	$V_{DD\text{-}25}$	$V_{DD\text{-}125}$
16-Bit ripple-carry adder	0.27	0.50
16-Bit carry select adder	0.32	0.53
16-Bit brent–kung adder	0.26	0.47
8-Bit array multiplier	0.36	0.59

energy consumption at 25 and 125 °C for a standard constant-V_{DD} and constant-f_s circuit operation are reported in Table 3.

The supply voltages providing minimum energy are observed in the subthreshold region, as listed in Table 3 [1,3]. The switching current in these ultra-low-voltage circuits is the subthreshold leakage current. Subthreshold leakage current is extremely sensitive to temperature fluctuations. A small change in the die temperature exponentially alters the subthreshold leakage current, as given by (5). The reversal in the temperature-dependent propagation-delay characteristics coupled with the high sensitivity of circuit speed to temperature fluctuations provides opportunities for reducing the energy consumption without degrading the clock frequency at elevated die temperatures in ultra-low supply voltage circuits.

4. Techniques for high-temperature energy reduction

In this section, the previously proposed conventional voltage scaling and body-bias techniques are briefly discussed. Two new temperature-adaptive dynamic voltage-tuning techniques for enhancing the high-temperature active-mode energy efficiency of circuits operating at ultra-low supply voltages are then introduced.

The operational load for an integrated circuit tends to have peak performance requirements followed by idle periods [5]. Maintaining the full computational capacity at all times, despite the reduction of the throughput requirements with variations of the workload, wastes significant amount of energy. Dynamic supply-voltage scaling technique exploits the variations in the computational workload by dynamically adjusting the supply voltage and the clock frequency of a synchronous system. The primary objective of the dynamic supply-voltage scaling technique is to provide high throughput during the execution of only the computation-intensive tasks, while saving energy during the rest of the time by lowering the supply voltage and the operating clock frequency. The dynamic voltage scaling technique is primarily aimed at reducing the active-mode power consumption of an integrated circuit.

Alternatively, the adaptive body-bias techniques utilize the bulk terminal to dynamically modify the threshold voltages of devices during circuit operation. Depending upon the polarity of the voltage difference between the source and the body terminals (V_{SB}), the threshold voltage can be either increased or decreased as compared to a zero-body-biased transistor. Device threshold voltages can be increased by applying reverse body bias in the standby mode in order to reduce the subthreshold leakage current produced by idle circuits. Furthermore, the dynamic supply-voltage scaling and adaptive body-bias techniques can also be used to compensate for the die-to-die and within-die process parameter variations, thereby enhancing the yield [5].

In ultra-low-voltage circuits, temperature gradients due to imbalanced switching activity within a die are typically small. The primary source of die temperature fluctuations in low-voltage circuits are the variations in the ambient temperature. Changes in the ambient temperature tend to affect all devices in an IC. At elevated die temperatures, the leakage currents as well as the circuit speed are enhanced. Increased leakage power, in turn, further enhances the heat dissipation and elevates the die temperature. This positive feedback between the die temperature, the leakage current, and the total power consumption significantly reduces the battery lifetime in portable devices, accelerates the degradation of the device/circuit reliability due to excessive heating, and can even cause thermal runaway in extreme environments despite the relatively low supply voltage. New temperature-adaptive design methodologies are, therefore, highly desirable to enhance the reliability and energy efficiency of ultra-low-voltage circuits operating at environments subjected to significant temperature fluctuations.

Integrated circuits are typically designed for guaranteed functionality at the estimated worst-case process and environmental parameter corners. In constant-V_{DD} and constant-f_s circuits optimized for minimum energy, the worst-case speed is observed at the lowest operating temperature. The lowest temperature therefore determines the achievable maximum clock frequency. As the die temperature increases, the circuits operate faster, thereby producing significant timing slack in the constant clock period.

In this paper, temperature-adaptive supply and threshold voltage-tuning techniques are proposed to dynamically adjust the circuit speed based on the die temperature. The primary objective of the proposed temperature-adaptive schemes is to lower the active-mode energy consumption by exploiting the excessive timing slack produced in the clock period at high die temperatures while maintaining a constant clock frequency across an entire die temperature spectrum. The objective is achieved by either dynamically scaling the power supply voltage or dynamically increasing the device threshold voltages through reverse body bias at elevated temperatures. The temperature-adaptive supply voltage tuning and the temperature-adaptive reverse body-bias techniques are presented in Sections 4.1 and 4.2, respectively.

4.1. Temperature-adaptive dynamic supply voltage scaling

The temperature-adaptive dynamic supply voltage scaling technique (TA-DVS) is presented in this section. All the primary components of power consumption in a CMOS circuit, namely dynamic switching, short circuit, and leakage power, are significantly reduced by scaling the supply voltage. The propagation delay of a circuit is also strongly dependent on the supply voltage [5]. Scaling the supply voltage reduces the power consumed by a circuit at the cost of degraded circuit performance.

The sum output (SUM [15]) of a 16-bit Brent–Kung adder operating at constant-V_{DD-25} and various temperatures is shown in Fig. 5. $V_{DD\text{-}25}$ for the Brent–Kung adder is 0.26 V, as listed in Table 2. The clock frequency is fixed at 32 kHz in a standard CMOS circuit (determined by the lowest operating temperature), the highest constant-f_s that can be maintained at all die temperatures, as listed in Table 2. The circuit operates faster at elevated temperatures, thereby producing excessive timing slack in the constant clock period, as shown in Fig. 5. At elevated temperatures, the total energy consumption increases due to the increase in the subthreshold leakage current [5]. The significant timing slack in the clock period can be exploited to reduce the active-mode energy consumption at elevated temperatures. With the proposed technique, the supply voltage of the circuit is dynamically scaled below $V_{DD\text{-}25}$, while maintaining the constant clock frequency of the circuit as the die temperature increases. The supply voltage of the circuit is tuned until the high-temperature circuit performance at the scaled supply voltage matches the low temperature circuit performance of the standard constant-V_{DD} and constant-f_s circuit operating at $V_{DD\text{-}25}$. Unlike the conventional work-load adaptive dynamic voltage scaling techniques [5–8], a new die temperature-adaptive dynamic voltage scaling technique is proposed in this paper for tuning the circuit supply voltage based on the fluctuations of the die temperature and the circuit speed.

A system with temperature-adaptive supply voltage-tuning capability is illustrated in Fig. 6. The low-temperature-V_{DD} and the target operating frequency (f_{target}) of the integrated circuit for achieving minimum energy consumption are determined at the lowest operating temperature according to the algorithm illustrated in Fig. 2. A ring oscillator providing a replica of the critical path of the entire integrated circuit is employed to track the fluctuations of the critical path propagation delay with the variations of the ambient temperature at a specific supply voltage. A relatively uniform temperature is assumed across the die with this technique. Note that the uniform die temperature assumption is typically satisfied with the ultra-low-voltage subthreshold logic circuits. The ring oscillator translates the variations in the die temperature to a specific clock frequency (f_{clock}) for a specific power supply voltage generated by the DC–DC converter. As the die temperature increases, the ring oscillator frequency (f_{clock}) also increases due to the enhanced gate overdrive voltages of the MOSFETs. The ring oscillator frequency is compared to the target clock frequency (f_{target}), generating a frequency error signal (f_{error}). The pulse width modulator using this error signal generates control signals for the DC–DC converter to either modify or maintain the output voltage. The power supply voltage is, thereby, dynamically tuned based on the variations of the die temperature using the closed loop feedback circuitry shown in Fig. 6.

The switching current in ultra-low-voltage circuits is the subthreshold leakage current. Supply-voltage scaling in the subthreshold regime reduces the I_{on}/I_{off} ratio [14]. Below a certain supply voltage, circuits with reduced I_{on}/I_{off} ratio fail to produce output signals with full rail-to-rail voltage swing [14]. The high-temperature signal swing of the sum output (SUM [15]) of a 16-bit Brent–Kung adder at various

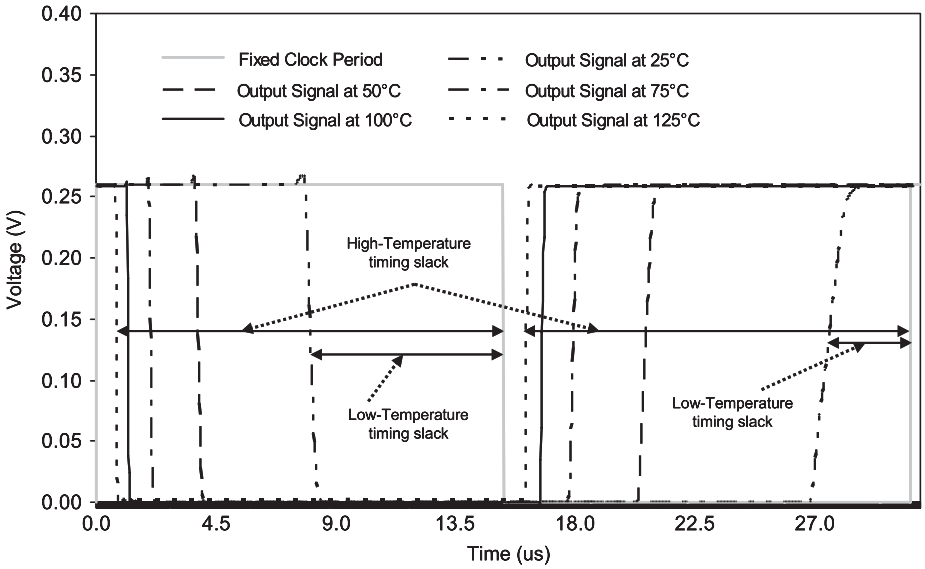

Fig. 5. Output signal (SUM [15]) of a 16-bit Brent–Kung adder operating at $V_{DD\text{-}25}$ (0.26 V) and various temperatures.

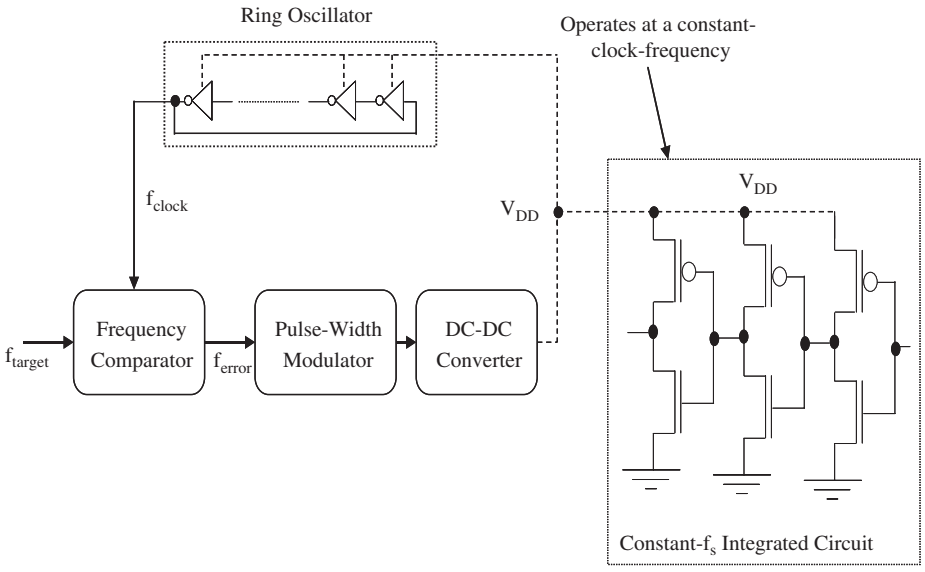

Fig. 6. Temperature-adaptive dynamic supply voltage scaling technique.

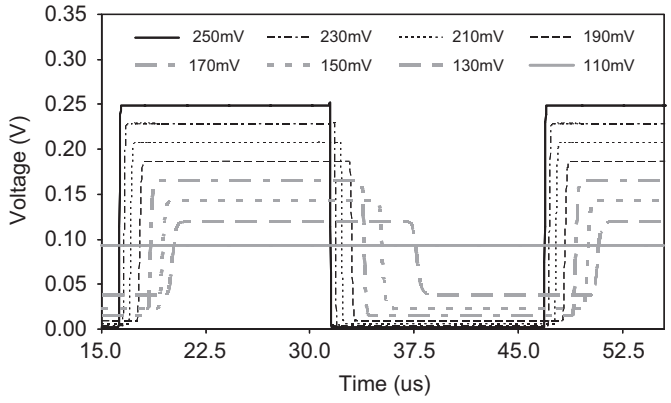

Fig. 7. Output signal swing of SUM [15] for a 16-bit Brent–Kung adder at various scaled supply voltages.

scaled supply voltages is shown in Fig. 7. As the supply voltage is scaled the signal swing starts to degrade, eventually causing malfunction at 110 mV, as shown in Fig. 7. The extent of temperature-adaptive dynamic voltage tuning that can be performed with the proposed technique is therefore limited by the acceptable degradation of the output signal voltage swing, as well as the circuit speed criterion determined by the lowest operating temperature. Supply voltages that achieve at least a $0.1V_{DD} \rightarrow 0.9V_{DD}$ output voltage swing for the entire temperature range are considered to be fully functional in this paper. Further reduction in the supply voltage lowers the high-temperature energy consumption at the cost of unacceptable degradation in the output voltage waveforms and the circuit noise margins.

For the standard constant-V_{DD} circuits designed for minimum energy at 125 °C (supply voltage fixed at $V_{DD\text{-}125}$), the worst-case circuit speed is similarly observed at the lowest temperature, as listed in Table 2. The maximum constant operating frequency that can be maintained for the entire die temperature spectrum is, therefore, determined by the lowest temperature in these standard circuits. Similar to the circuits operating at $V_{DD\text{-}25}$, as the die temperature increases, the propagation delays are significantly reduced in a circuit that operates at $V_{DD\text{-}125}$. With the proposed temperature-adaptive supply voltage-tuning technique, without violating the constant-clock-frequency requirement, the speed of these circuits at elevated temperatures can be dynamically adjusted for exploiting the enhanced timing slack in the clock period. The temperature-adaptive supply voltage-tuning technique thereby further reduces the high-temperature energy consumption as compared to even a standard constant-V_{DD} circuit designed for minimum energy operation at 125 °C.

The high-temperature energy reduction observed with the proposed temperature-adaptive supply voltage-tuning technique in circuits optimized for minimum energy at 125 °C is illustrated next for a 16-bit Brent–Kung adder. $V_{DD\text{-}125}$ for the Brent–Kung adder is 0.47 V, as listed in Table 2. The frequency of the circuit is fixed at 2.7 MHz, the highest constant-f_s that can be maintained at all die temperatures for $V_{DD} = 0.47$ V. At 125 °C, however, this adder is actually capable of operating at a clock frequency of up to 8.87 MHz with this supply voltage. In a standard CMOS circuit, since the V_{DD} and frequency are fixed at 0.47 V and 2.7 MHz, respectively, the available clock period is essentially under-utilized at elevated temperatures.

With the proposed technique, the supply voltage of the circuit is further scaled at elevated temperatures ($V_{DD} < V_{DD\text{-}125}$) to exploit the excessive slack observed in the clock period while maintaining the functionality at 2.7 MHz. The high-temperature maximum clock frequency and energy consumption of a Brent–Kung adder is listed in Table 4 for various power supply voltages. As listed in

Table 4, at 125 °C the supply voltage can be scaled from 0.47 V ($V_{DD\text{-}125}$) to 0.39 V while maintaining the clock frequency at 2.7 MHz. Scaling the supply voltage reduces the high-temperature energy consumption from 0.148 pJ (the minimum energy achievable with V_{DD} fixed at $V_{DD\text{-}125} = 0.47$ V) to 0.108pJ ($V_{DD} = 0.39$ V), as listed in Table 4. Supply voltage scaling at elevated temperatures thereby significantly lowers the energy consumption below the minimum energy achievable with the standard constant-V_{DD} and constant-f_s circuits.

The propagation delays of standard CMOS circuits operating at $V_{DD\text{-}25}$ and $V_{DD\text{-}125}$ are compared with high-temperature propagation delays of circuits based on the TA-DVS technique in Tables 5 and 6, respectively. The scaled supply voltages of the TA-DVS circuits listed in Tables 5 and 6 are the minimum V_{DD} that achieves at least a $0.1V_{DD} \rightarrow 0.9V_{DD}$ output voltage swing while maintaining the low-temperature clock frequency at elevated temperatures. As listed in Table 5, the scaled supply voltages that maintain the clock frequency at high temperatures are 29.6% (ripple-carry adder) to 38.9% (array multiplier) lower as compared to the supply voltages required by the standard constant-V_{DD} circuits for achieving minimum energy at 25 °C ($V_{DD\text{-}25}$). Similarly, with the proposed technique, the supply voltage at elevated temperatures can be scaled by up to 17% (Brent–Kung adder) as compared to the supply voltage required by the standard constant-V_{DD} circuits for achieving minimum energy at 125 °C ($V_{DD\text{-}125}$), as listed in Table 6.

The normalized high-temperature energy consumption of the standard constant-V_{DD} circuits and the circuits based on the TA-DVS technique are listed in Table 7. The high-temperature energy consumption is reduced by up to 40% (carry select adder) and 28% (Brent–Kung adder) with the temperature-adaptive dynamic supply voltage-tuning technique as compared to the standard constant-V_{DD} circuits providing minimum energy at 25 °C ($V_{DD\text{-}25}$) and 125 °C ($V_{DD\text{-}125}$), respectively.

Table 4
Max-f_s and energy consumption for a brent–kung adder at different supply voltages ($t = 125$ °C)

V_{DD} (V)	Maximum. frequency at 125 °C (MHz)	Energy consumption at 125 °C (pJ)
0.47 ($V_{DD\text{-}125}$)	8.87	0.148
0.45	6.86	0.138
0.43	5.45	0.127
0.41	4.18	0.117
0.39	3.20	0.108
0.37	2.40	0.098

The target clock frequency at $V_{DD\text{-}125}$ is 2.7 MHz. At elevated temperatures, the supply voltage can be scaled while maintaining the clock frequency.

4.2. Temperature-adaptive body bias

An alternative voltage-tuning technique based on temperature-adaptive body bias (TA-BB) is presented in this section. Similar to the dependence on the supply

Table 5
Propagation delay comparison of constant-V_{DD} circuits at $V_{DD\text{-}25}$ and circuits with TA-DVS capability

Circuits in a 180 nm CMOS technology	Standard constant voltage operation at $V_{DD\text{-}25}$			SVM	
	V_{DD} (V)	PD		V_{DD} (V)	PD
		25 °C	125 °C		125 °C
16-Bit ripple carry adder	0.27	15.59	1.48	0.19	5.05
16-Bit carry select adder	0.32	3.40	0.32	0.20	1.83
16-Bit Brent–Kung adder	0.26	10.10	0.81	0.17	3.21
8-Bit array multiplier	0.36	3.89	0.47	0.22	3.85

SVM: supply voltages that match the high-temperature performance of the TA-DVS circuits with the low-temperature performance of the standard constant-supply voltage circuits. PD: propagation delay in micro-seconds.

Table 6
Propagation delay comparison of constant-VDD circuits at $V_{DD\text{-}125}$ and circuits with TA-DVS capability

Circuits in a 180 nm CMOS technology	Standard constant voltage operation at $V_{DD\text{-}125}$			SVM	
	V_{DD} (V)	PD		V_{DD} (V)	PD
		25 °C	125 °C		125 °C
16-Bit ripple-carry adder	0.50	0.166	0.068	0.43	0.149
16-Bit carry select adder	0.53	0.056	0.023	0.45	0.055
16-Bit brent–kung adder	0.47	0.127	0.043	0.39	0.117
8-Bit array multiplier	0.59	0.065	0.034	0.52	0.063

voltage, the propagation delay of a circuit is also strongly dependent on the device threshold voltages [5]. The absolute values of threshold voltages degrade as the temperature increases, thereby simultaneously enhancing the circuit speed and the subthreshold leakage currents at elevated temperatures [5,10]. In ultra-low-voltage circuits exhibiting reversed temperature dependence, the threshold voltage of devices is dynamically increased through reverse body bias at elevated temperatures to exponentially reduce the leakage current without degrading the clock frequency. The device threshold voltages are increased until the high-temperature circuit performance of the TA-BB circuit matches the worst-case circuit performance of a standard-zero-body-biased circuit operating at a constant-V_{DD}. Unlike the conventional body-bias techniques aimed at altering the device threshold voltages based on variations of the workload and circuit activity, the proposed TA-BB technique alters the threshold voltages of the devices based on fluctuations of the die temperature and the circuit speed.

Table 7
Normalized energy savings with the temperature-adaptive voltage scaling scheme

Circuits in a 180 nm CMOS technology	High-temperature (125 °C) energy consumption			
	$V_{DD\text{-}25}$	SVM	$V_{DD\text{-}125}$	SVM
16-Bit ripple carry adder	1.00	0.69	1.00	0.77
16-Bit carry select adder	1.00	0.60	1.00	0.76
16-Bit Brent–Kung adder	1.00	0.64	1.00	0.72
8-Bit array multiplier	1.00	0.62	1.00	0.79

SVM: supply voltages that match the high-temperature performance of the TA-DVS circuits with the low-temperature performance of the standard constant-supply voltage circuits.

The TA-BB technique is illustrated in Fig. 8. Integrated circuits with the TA-BB technique operate with a constant supply voltage. The supply voltage and the target operating frequency (f_{target}) are determined according to the algorithm illustrated in Fig. 2. For a minimum energy consumption at 25 °C (125 °C), the supply voltage of the circuit is fixed at $V_{DD\text{-}25}$ ($V_{DD\text{-}125}$). A ring oscillator providing a replica of the critical path of the entire integrated circuit translates the die temperature to a specific clock frequency (f_{clock}) for a specific set of body-bias voltages produced by the PMOS and NMOS body-bias generators. Note that a relatively uniform temperature is assumed across the die with this technique. The ring oscillator frequency (f_{clock}) is compared with the target operating frequency (f_{target}) and a frequency error signal (f_{error}) is generated. Using this error signal, the body-bias generators either modify or maintain the body-bias voltages applied to the devices in the integrated circuit. The device threshold voltages are, thereby, dynamically tuned based on die temperature variations for maintaining a constant circuit speed across the entire die temperature spectrum.

The propagation delays of standard zero-body-biased circuits are compared with the high-temperature propagation delays of circuits based on the TA-BB technique operating at $V_{DD\text{-}25}$ and $V_{DD\text{-}125}$ in Tables 8 and 9, respectively. As listed in Table 8, the applicable high-temperature reverse body-bias voltages are 0.40 V (array multiplier) to 0.47 V (Brent–Kung adder) with the TA-BB technique, while maintaining the same clock-frequency as compared to the standard-zero-body-biased circuits operating at $V_{DD\text{-}25}$. Similarly, the applicable high-temperature reverse body-bias voltages are 0.21 V (array multiplier) to 0.25 V (Brent–Kung adder) with the TA-BB technique for maintaining the same clock frequency as compared to the standard-zero-body-biased circuits operating at $V_{DD\text{-}125}$, as listed in Table 9.

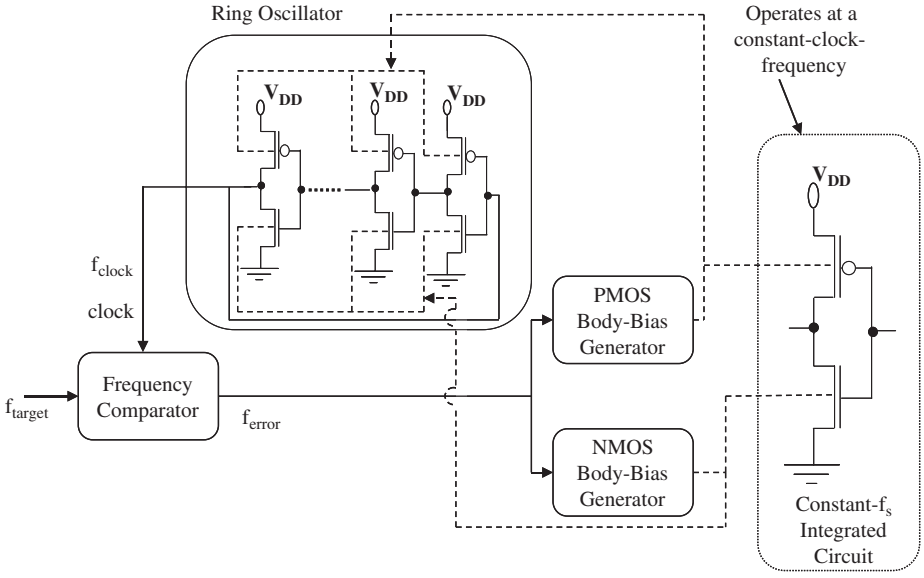

Fig. 8. Temperature-adaptive body-bias technique. V_{DD}: standard constant-supply voltage providing minimum energy ($V_{DD\text{-}25}$ or $V_{DD\text{-}125}$).

The normalized high-temperature energy consumption of the standard-zero-body-biased circuits and the circuits based on the TA-BB technique are listed in Table 10. The high-temperature energy consumption is increased by up to 6× (ripple carry adder) and 1.2× (ripple carry and Brent–Kung adder) with the temperature-adaptive reverse body-bias technique as compared to the standard-zero-body-biased circuits providing minimum energy at 25 °C ($V_{DD\text{-}25}$ and $|V_{SB}| = 0$) and 125 °C ($V_{DD\text{-}125}$ and $|V_{SB}| = 0$), respectively.

The reason for the higher energy consumption at elevated temperatures in circuits with the TA-BB technique is illustrated here with a p-channel MOSFET in a 180 nm CMOS technology. The switching current at ultra-low power-supply voltages is the subthreshold leakage current. A p-channel MOSFET operating in the subthreshold regime with the drain biased at 0V and the gate and source terminals biased at 0.27 V (the supply voltage providing minimum energy for a ripple-carry adder at 25 °C, as listed in Table 3) is shown in Fig. 9. The currents observed at different terminals of this PMOS transistor for various body-bias voltages (V_{BB}) are listed in Table 11 along with the total power consumption of the device.

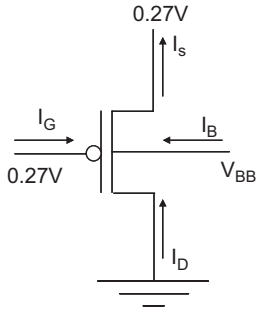

Fig. 9. A PMOS device in the TSMC 180 nm CMOS technology. The gate and source terminals are biased at 0.27 V. Temperature = 125 °C. The device is reverse body biased by applying a voltage higher than 0.27 V to the body terminal.

Table 8
Propagation delay comparison of zero-body-biased circuits operating at $V_{DD\text{-}25}$ and circuits with TA-BB capability

Circuits in a 180 nm CMOS technology	Standard constant voltage operation at V_{DD-25}			RBB	
	$\|V_{SB}\|$ (V)	PD		$\|V_{SB}\|$ (V)	PD
		25 °C	125 °C		125 °C
16-Bit ripple-carry adder	0.00	15.59	1.48	0.44	14.87
16-Bit carry select adder	0.00	3.40	0.32	0.45	3.32
16-Bit brent–kung adder	0.00	10.10	0.81	0.47	10.02
8-Bit array multiplier	0.00	3.89	0.47	0.40	3.80

RBB: reverse body-bias voltages that match the high-temperature performance of the TA-BB circuits with the low-temperature performance of the standard-zero-body-biased. PD: propagation delay in micro-seconds.

Table 9
Propagation delay comparison of zero-body-biased circuits operating at $V_{DD\text{-}125}$ and circuits with TA-BB capability

Circuits in a 180 nm CMOS Technology	Standard constant voltage operation at $V_{DD\text{-}125}$			SVM	
	$\|V_{SB}\|$ (V)	PD		$\|V_{SB}\|$ (V)	PD
		25 °C	125 °C		125 °C
16-Bit ripple carry adder	0.00	0.166	0.068	0.23	0.161
16-Bit carry select adder	0.00	0.056	0.023	0.24	0.055
16-Bit Brent–Kung adder	0.00	0.127	0.043	0.25	0.123
8-Bit array multiplier	0.00	0.065	0.034	0.21	0.063

Table 10
Normalized energy reduction with the temperature-adaptive voltage scaling scheme

Circuits in a 180 nm CMOS technology	High-temperature (125 °C) energy consumption			
	$V_{DD\text{-}25}$	RBB	$V_{DD\text{-}125}$	RBB
16-Bit ripple carry adder	1.00	6.02	1.00	1.22
16-Bit carry select adder	1.00	3.94	1.00	1.12
16-Bit Brent–Kung adder	1.00	5.52	1.00	1.22
8-Bit array multiplier	1.00	3.41	1.00	1.08

Table 11
Post-layout current measured at the different terminals of the PMOS device for various body-bias voltages

V_{BB} (V)	$\lvert V_{SB}\rvert$ (V)	I_D (pA)	I_S (pA)	I_G (pA)	I_B (pA)	Device total power consumption (pW)
0.27	0.00	−397.55	−87.92	0.00	309.63	107.34
0.32	0.05	−368.15	179.09	0.00	547.24	126.76
0.37	0.10	−348.95	253.70	0.00	602.64	154.48
0.42	0.15	−336.31	279.31	0.00	615.62	183.15
0.47	0.20	−327.95	290.77	0.00	618.72	212.29
0.52	0.25	−322.38	297.14	0.00	619.52	241.92
0.57	0.30	−318.64	301.14	0.00	619.78	271.97
0.62	0.35	−316.13	303.79	0.00	619.92	302.33
0.67	0.40	−314.43	305.60	0.00	620.03	332.91

Applying reverse body-bias increases the device threshold voltage, thereby reducing the subthreshold leakage current [5]. Applying reverse body bias, however, also increases the junction leakage currents due to the enhanced band-to-band tunneling [5]. As listed in Table 11, even for a small reverse body-bias voltage ($|V_{SB}| = 0.05$ V), the leakage current through the body diodes increases by up to 76.7% (from 309.63 to 547.24 pA) as compared to a zero-body-biased transistor. For relatively high reverse body-bias voltages required in circuits with the TA-BB technique ($|V_{SB}|$ ranging from 0.21 to 0.47 V), the increase in the body current dominates the reduction in the subthreshold leakage current, thereby increasing the total power consumed by the device, as listed in Table 11.

5. Effectiveness of the temperature-adaptive voltage-tuning schemes

The effectiveness of the proposed temperature-adaptive schemes for lowering the active-mode energy consumption is evaluated in this section. The energy consumptions with the TA-DVS and TA-BB design methodologies are compared in Section 5.1. The impact of the process parameter and environmental variations on the reliability of the proposed schemes is evaluated in Section 5.2.

5.1. Characteristics of the temperature-adaptive schemes

The tradeoffs in the implementation of the temperature-adaptive voltage-tuning schemes in circuits optimized for minimum energy consumption are presented in this section. The percent energy reduction provided with the two temperature-adaptive schemes is compared to the standard CMOS circuits operating at V_{DD-25} in Table 12. The high-temperature energy efficiency is significantly enhanced by up to 40% with the temperature-adaptive supply voltage-tuning technique, as listed in Table 12. Alternatively, the energy consumption increases by up to 6× with the temperature-adaptive reverse body-bias technique as compared to the standard-zero-body-bias circuits operating at $V_{DD\text{-}25}$. TA-BB technique is therefore not effective for enhancing the high-temperature energy efficiency in ultra-low-voltage subthreshold logic circuits.

Table 12
Percent energy reduction with the temperature-adaptive voltage tuning schemes

Circuits in a 180 nm CMOS technology	Percent energy reduction (%)	
	TA-DVS	TA-BB
16-Bit ripple-carry adder	31	−502
16-Bit carry select adder	40	−294
16-Bit brent–kung adder	36	−452
8-Bit array multiplier	38	−241

The proposed temperature-adaptive schemes can be implemented in a standard n-well or p-well CMOS technology. The temperature-adaptive dynamic supply voltage-tuning technique requires an energy-efficient high-resolution voltage scaling power supply for producing the ultra-low supply voltages. The energy overheads related with modifying the voltage of the power distribution network and with tuning the power supply voltage should be further investigated to evaluate the net energy reduction provided with the proposed temperature-adaptive supply voltage-tuning technique.

5.2. Impact of the process parameter and supply-voltage variations

Subthreshold logic circuits are highly sensitive to variations in the process parameters, the supply voltage, and the operating temperature [1,4,5]. Both the performance and the energy consumption of integrated circuits are altered due to the fluctuations of the circuit parameters [5,17,18]. The impact of the parameter variations on the proposed temperature-adaptive voltage-tuning techniques is evaluated in this section. As described in Section 5.1, only the TA-DVS technique is effective in enhancing the high-temperature energy efficiency in ultra-low-voltage subthreshold logic circuits. Therefore, only the TA-DVS technique is evaluated in this section under parameter variations.

Random and systematic fluctuations in the channel length (L_{GATE}), the doping concentration (N_{CH}), and the gate-oxide thickness (T_{OX}) cause variations in the threshold voltage of a MOSFET. Fluctuation in the threshold voltage alters the performance and the power consumption (both dynamic and leakage power consumption) of a circuit. In this paper, the variations in the performance and the energy consumption due to the process variations in the channel length (L_{GATE}), the doping concentration (N_{CH}), and gate-oxide thickness (T_{OX}) are evaluated. Each parameter is assumed to have an independent normal Gaussian statistical distribution with a three-sigma variation of 10% [18].

Another important source of noise in CMOS integrated circuits is the power supply noise [5]. Integrated circuits are typically designed to meet performance specifications at a voltage 10% lower than the nominal supply voltage to account for the supply-voltage variations [5]. In this paper, the supply voltage is assumed to have an independent normal Gaussian statistical distribution with a three-sigma variation of 10%.

Monte-Carlo simulations (30 simulations) are run to evaluate the performance and energy consumption fluctuations in circuits with the TA-DVS technique. The delay versus energy consumption plots for the 16-bit ripple-carry adders operating at $V_{DD\text{-}25}$ and the optimized high-temperature supply voltage with the TA-DVS technique are shown in Fig. 10. $V_{DD\text{-}25}$ for the ripple-carry adder is 0.27 V (as listed in Table 3). In the presence of variations, the high-temperature (125 °C) energy consumption of standard constant-V_{DD} ripple carry adders operating at $V_{DD\text{-}25}$ ranges from 1.54 to 1.84 pJ, as shown in Fig. 10. Alternatively, ripple carry adders with TA-DVS have lower energy consumption at 125 °C (energy consumption ranges from 1.17 to 1.28 pJ) in the presence of process parameter and supply-voltage variations, as shown in Fig. 10. Furthermore, the high-temperature propagation delay of ripple carry adders with TA-DVS (propagation-delay range is from 4.85 to 5.41 μs, as shown in Fig. 10) is smaller as compared to the low-temperature performance of the standard constant-supply-voltage ripple carry adder (propagation delay at $V_{DD} = V_{DD\text{-}25}$ and temperature = 25 °C is 15.59 μs, as listed in Table 5). The smaller high-temperature propagation delay in circuits with the TA-DVS technique indicates that there is sufficient timing slack in the constant clock period to allow temperature-adaptive voltage scaling even in the presence of variations.

The mean and standard deviation of the high-temperature (125 °C) energy consumption of the standard constant-V_{DD} ripple-carry adder circuits operating at $V_{DD\text{-}25}$ are 1.67 pJ and 84.9 fJ, respectively. The three standard deviation (3-sigma) offset of the *lowest* energy consumption in these circuits is (mean−3 standard deviation) 1.41 pJ. Alternatively, the mean and the standard deviation of the high-temperature (125 °C) energy consumption of the ripple carry adders with TA-DVS are 1.22 pJ and 25.4 fJ, respectively. The 3-sigma offset of the *highest* energy consumption in the circuits with the TA-DVS technique (mean + 3 standard deviation) is 1.29 pJ. These results indicate that the highest possible energy consumption of a circuit with TA-DVS is still lower than the lowest possible energy consumption of a standard constant-V_{DD} circuit when the parameter fluctuations are considered. The effectiveness of the proposed temperature-adaptive dynamic voltage scaling technique for enhancing the high-temperature energy efficiency is therefore maintained in the presence of process parameter and supply voltage variations.

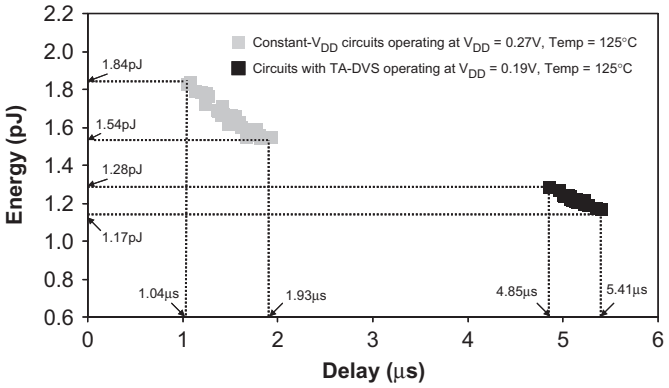

Fig. 10. Delay versus energy consumption plots for the 16-bit ripple carry adders operating at $V_{DD\text{-}25}$ and at the optimized high-temperature supply voltage with the TA-DVS in the presence of process parameter and supply voltage variations. N_{CH}, L_{GATE}, T_{OX}, and V_{DD} are assumed to have independent normal Gaussian statistical distributions with a three-sigma variation of 10%.

6. Conclusions

Gate overdrive variation with temperature dominates the speed characteristics of circuits operating at ultra-low-voltages. In ultra-low power-supply-voltage CMOS circuits, the circuit speed is enhanced with increased temperature. The excessive timing slack observed in the clock period at elevated temperatures provides new opportunities to lower the active-mode energy consumption without violating the constant-clock-frequency requirement. Temperature-adaptive dynamic supply-voltage-tuning technique is proposed in this paper to reduce the high-temperature energy consumption of ultra-low-voltage subthreshold logic circuits.

The temperature-adaptive supply-voltage scaling technique dynamically adjusts the power supply voltage of a circuit based on the die-temperature fluctuations. The high-temperature energy consumed with the temperature-adaptive voltage scaling technique is reduced by up to 40% as compared to the minimum energy achievable with the standard constant-V_{DD} and constant-frequency circuits. An alternative technique based on the temperature-adaptive reverse body-bias that dynamically tunes the threshold voltages of the devices based on the fluctuations of the die temperature and the circuit speed is also evaluated in this paper. Temperature-adaptive dynamic supply voltage-tuning technique is shown to be very

effective to reduce the high-temperature energy consumption without degrading the clock frequency in subthreshold logic circuits operating at ultra-low power-supply voltages.

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