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# TEMPERATURE-ADAPTIVE ENERGY REDUCTION TECHNIQUES FOR NANO-CMOS CIRCUITS DISPLAYING REVERSED TEMPERATURE DEPENDENCE

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Temperature dependent propagation delay characteristics of CMOS circuits will experience a complete reversal in the near future. Contrary to the older technology generations, the speed of circuits in a 32 nm CMOS technology is enhanced when the temperature is increased at the nominal supply and threshold voltages. The enhancement of circuit speed provides new opportunities to lower the energy consumed by active circuits at elevated temperatures. Temperature-adaptive supply and threshold voltage tuning techniques are proposed in this paper to reduce the high temperature energy consumption without degrading the clock frequency in the active mode. Results indicate that the energy consumption can be lowered by up to 21% by dynamically scaling the supply voltage at elevated temperatures. An alternative technique based on temperature-adaptive reverse body-bias exponentially reduces the leakage currents as well as the parasitic junction capacitances of the MOSFETs. The temperature-adaptive threshold voltage tuning through reverse body-bias yields an active mode energy reduction by up to 29.8% as compared to the standard zero-body-biased circuits at high temperatures.

*Keywords*: Adaptive body-bias; dynamic voltage scaling; hot spots; reversed temperature dependence; supply voltage tuning; temperature variations; threshold voltage tuning.

## 1. Introduction

Process and environment parameter variations in scaled CMOS technologies are posing greater challenges in the design of reliable integrated circuits. Because of the imbalanced utilization and diversity of circuitry, temperature can vary significantly from one die area to another.[1] Furthermore, environmental temperature fluctuations can cause significant variations in the die temperature. For example, electronic systems mounted on automobile engines operate at a temperature range

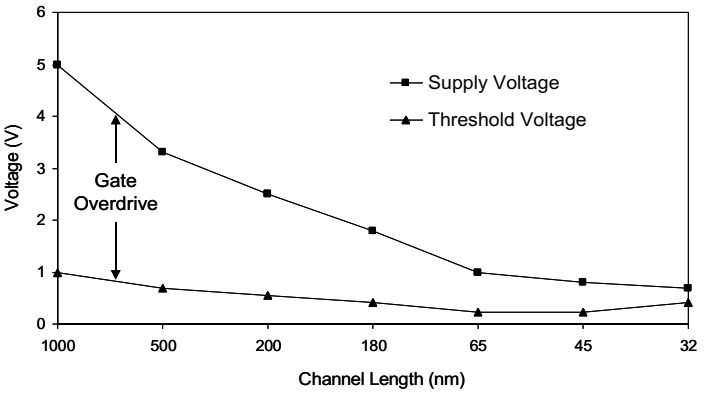


Fig. 1. The circuit power supply and MOSFET threshold voltages at different CMOS technologies. (*Source*: R. Kumar and V. Kursun, Reversed temperature dependent propagation delay characteristics in nanometer CMOS circuits, *IEEE Trans. Circuits Syst. II* **53** (2006) 1078–1082.)

from −40°C to 150°C.[2] Variations in the die temperature affect the device and wire characteristics thereby altering the performance of integrated circuits.

The supply and threshold voltage scaling trends are shown in Fig. 1.[3] The supply voltage in a new technology generation is determined based on the target clock frequency, the power consumption budget, and the device reliability requirements.[3,4] Scaling the device dimensions strengthens the electric fields between the device terminals while lowering the parasitic capacitances, thereby enhancing the speed of CMOS integrated circuits. The speed of a circuit can be further enhanced by scaling the threshold voltages. Due to the subthreshold leakage current constraints, however, the threshold voltages are scaled at a much slower rate as compared to the supply voltage. The supply voltage to threshold voltage ratio is reduced with each new technology generation. The variation of the threshold voltage therefore plays an increasingly important role in determining the MOSFET drain current variations when the temperature fluctuates. As discussed in Ref. 3, a complete reversal in the temperature dependent speed characteristics of CMOS circuits will occur in the near future.

Dynamic voltage scaling technique is primarily used for reducing the active mode power consumption of an integrated circuit by exploiting the variations in the computational workload.[4–6] Alternatively, adaptive body-bias technique reduces both the active and the standby mode power consumption by dynamically adjusting the device threshold voltages depending on the variations of the workload and the circuit activity.[4,7–11] In this paper, new temperature-adaptive dynamic supply and threshold voltage tuning techniques are proposed to reduce the energy consumption of active CMOS circuits at elevated temperatures. In a circuit that exhibits reversed temperature dependence, the high temperature energy efficiency can be enhanced, without degrading the clock frequency, either by dynamically scaling the supply voltage or by reverse body-biasing the devices in the circuit. The optimum power supply and body-bias voltages that lower the energy consumption without

degrading the circuit speed at increased temperatures are identified in this paper for circuits in a 32 nm CMOS technology. The active mode energy savings provided with the different temperature-adaptive dynamic voltage tuning techniques are compared.

The paper is organized as follows. The effects of temperature fluctuations on the device and circuit characteristics at the nominal supply and threshold voltages are examined in Sec. 2. The new temperature-adaptive supply and threshold voltage scaling techniques for reducing the energy consumed at high die temperatures are described in Sec. 3. The energy reduction observed with the temperature-adaptive design methodologies are compared in Sec. 4. Finally, some conclusions are provided in Sec. 5.

## 2. Device and Circuit Behavior Under Temperature Fluctuations

The effects of temperature fluctuations on the device and circuit characteristics are reviewed in this section. An increase in the die temperature degrades the absolute values of threshold voltage, carrier mobility, and saturation velocity of MOSFETs.[3,12–14] The saturation velocity is typically a weak function of temperature.[13] Threshold voltage degradation with temperature tends to enhance the drain current because of the increase in gate overdrive $|V_{GS} - V_t|$. Alternatively, degradation in carrier mobility tends to lower the MOSFET drain current. Effective variation of MOSFET drain current is determined by the variation of the dominant device parameter when the temperature fluctuates.[3] Temperature fluctuation induced gate overdrive and carrier mobility variations at the nominal supply and threshold voltages for devices in a 32 nm CMOS technology[15] are listed in Table 1. Variation of the MOSFET drain current ($I_{DS}$) with the supply voltage and the temperature is shown in Fig. 2.

In older technology generations with higher supply to threshold voltage ratio, the variation of the carrier mobility dominates the MOSFET current when the temperature fluctuates at the nominal supply and threshold voltages.[3,14] The MOSFET drain current and the circuit speed are, therefore, reduced following the degradation of carrier mobility when the temperature is increased at the nominal voltages.[3] The reduction in the supply voltage to threshold voltage ratio with technology scaling,

Table 1. Gate overdrive and carrier mobility variations at the nominal supply and threshold voltages.*

| 32 nm CMOS technology | Gate overdrive (V) | | Carrier mobility ($\times 10^{-3}$ m$^2$/Vs) | |
|---|---|---|---|---|
| | PMOS | NMOS | PMOS | NMOS |
| 25°C | −0.286 | 0.275 | 3.85 | 17.00 |
| 125°C | −0.399 | 0.398 | 2.73 | 11.24 |
| Variation (%) | 39.63 | 44.85 | −29.22 | −33.85 |

*$|V_{GS}| = V_{DD,nom} = 0.7$ V, PMOS $V_{t0} = -0.41$ V, NMOS $V_{t0} = 0.42$ V.

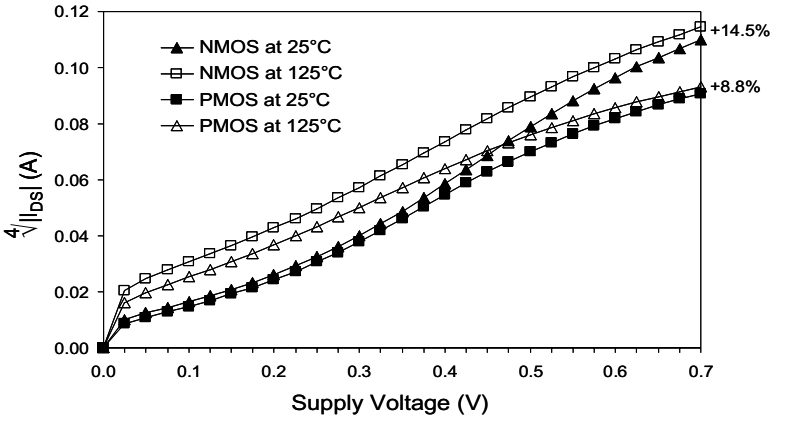


Fig. 2. Variations of MOSFET drain current with supply voltage and temperature in a 32 nm CMOS technology. $|V_{DS}| = |V_{GS}| = V_{DD}$. PMOS $V_{t0} = -0.41$ V. NMOS $V_{t0} = 0.42$ V.

as illustrated in Fig. 1, enhances the rate of increase of the gate overdrive with the increased temperature. As listed in Table 1, the temperature fluctuation induced variations of gate overdrive are more significant as compared to the fluctuations of carrier mobility for the devices in this 32 nm CMOS technology. The enhanced sensitivity of the gate overdrive to the fluctuations of the temperature alters the device and circuit characteristics in deeply scaled CMOS technologies. Contrary to the devices in older technology generations, MOSFET drain current increases when the temperature is increased at the nominal voltages in this 32 nm CMOS technology, as shown in Fig. 2.

The propagation delay variations with the temperature for the test circuits (designed for equal low-to-high and high-to-low propagation delays at the worst-case lowest temperature) operating at the nominal supply and threshold voltages are shown in Fig. 3. Contrary to the circuits in older technology generations,[3] circuit speed increases by up to 18.7% when the temperature is increased from 25°C to 125°C at the nominal voltages. The reversal in the temperature dependent propagation delay characteristics provides new opportunities for reducing the energy consumption without degrading the speed of CMOS circuits at high die temperatures.

## 3. Techniques for High Temperature Energy Reduction

Reducing power dissipation is a primary objective in the design of digital integrated circuits.[4,9] Power consumption of CMOS circuits can be lowered by employing several techniques as described in Refs. 4–11. In this section, the different sources of power consumption along with the previously proposed conventional voltage scaling and body-bias techniques are briefly discussed. The new temperature-adaptive dynamic voltage tuning techniques are then introduced.

The two primary sources of power dissipation in CMOS circuits are the static power, which results from leakage currents of the MOSFETs, and the dynamic

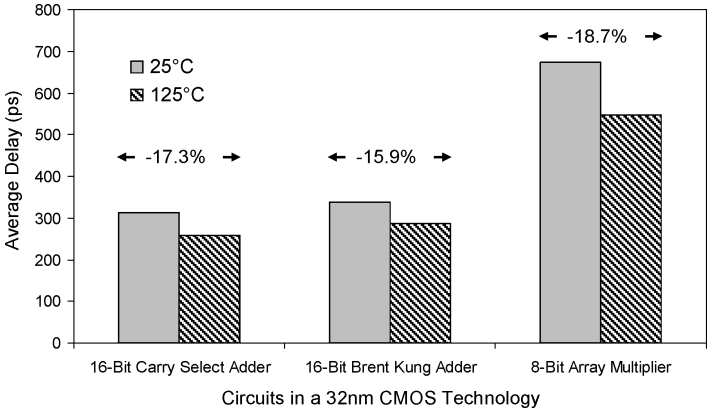


Fig. 3. Percent delay variation with temperature for circuits operating at the nominal supply and threshold voltages (PMOS $V_{t0} = -0.41\,\mathrm{V}$, NMOS $V_{t0} = 0.42\,\mathrm{V}$, and $V_{DD,nom} = 0.7\,\mathrm{V}$).

power, which results from the switching activity. The subthreshold leakage current produced by a MOSFET is[4]

$$I_{leak} = \frac{\mu W_{eff} C_{OX}}{L_{eff}} V_T^2 e^{\frac{|V_{GS}|-|V_t|}{nV_T}} \left(1 - e^{\frac{-|V_{DS}|}{V_T}}\right), \tag{1}$$

where $I_{leak}$, $\mu$, $W_{eff}$, $C_{OX}$, $L_{eff}$, $V_t$, $V_T$, $V_{GS}$, $V_{DS}$, and $n$ are the subthreshold leakage current, carrier mobility, effective transistor width, oxide capacitance per unit area, effective channel length, threshold voltage, thermal voltage, gate-to-source voltage, drain-to-source voltage, and subthreshold swing coefficient, respectively.

Absolute value of the threshold voltage degrades as the temperature increases.[4,12–14] Degradation of the threshold voltage and the enhancement of the thermal voltage exponentially increase the subthreshold leakage current at higher temperatures, as given by (1). The total leakage energy consumed by an integrated circuit is, therefore, significantly increased at elevated temperatures. The normalized leakage energy profiles of the circuits in this 32 nm CMOS technology are shown in Fig. 4 for different temperatures. The leakage energy of each circuit is normalized to the leakage energy consumed by the corresponding circuit at room temperature (25°C). The leakage energy consumed at 125°C is up to 9.4× higher as compared to the leakage energy at 25°C, as shown in Fig. 4.

The operational load for an integrated circuit tends to have peak performance requirements followed by idle periods.[4] Maintaining the full computational capacity at all times, despite the reduction of the throughput requirements with the variations of the workload, wastes significant amount of energy. Dynamic supply voltage scaling technique exploits the variations in the computational workload by dynamically adjusting the supply voltage and the clock frequency of a synchronous system. The primary objective of the workload-adaptive dynamic supply voltage scaling technique is to provide high throughput during the execution of only the computation-intensive tasks while saving energy during the rest of the time

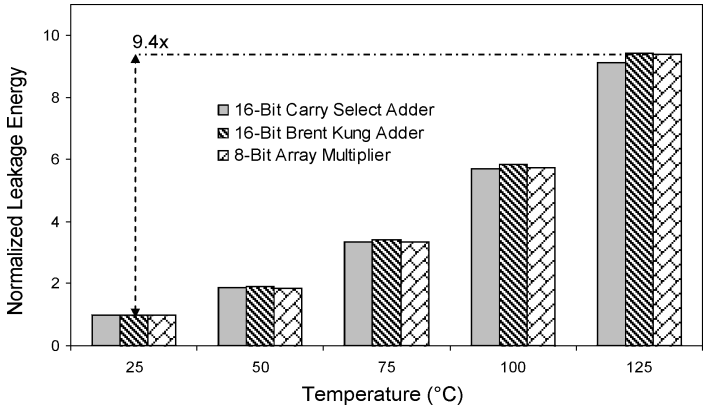


Fig. 4. Normalized leakage energy for circuits operating at the nominal supply and threshold voltages. The operating frequency of each circuit is maintained constant at different temperatures.

by lowering the supply voltage and the operating clock frequency. The workload-adaptive dynamic voltage scaling technique is primarily aimed at reducing the active mode power consumption of an integrated circuit.

Alternatively, the adaptive body-bias techniques utilize the bulk terminal to dynamically modify the threshold voltages of the devices during circuit operation. Depending upon the polarity of the voltage difference between the source and the body terminals ($V_{SB}$), the threshold voltage can be either increased or decreased as compared to a zero body-biased transistor. Device threshold voltages can be increased by applying reverse body-bias in the standby mode in order to reduce the subthreshold leakage current produced by idle circuits.[4] Furthermore, the dynamic supply voltage scaling and the adaptive body-bias techniques can also be used to compensate for the die-to-die and within-die process parameter variations, thereby enhancing the yield.[4]

Integrated circuits are designed for functionality at the worst-case process and environmental parameter corners. From a speed perspective, the worst-case temperature has been the highest operating temperature in the older technology generations.[3,4] Integrated circuits are, therefore, designed to satisfy the clock period timing requirements at the highest operating temperature. Alternatively, in deeply scaled CMOS technologies, the worst-case is shifted to the lowest operating temperature due to the determination of the propagation delay characteristics primarily by the gate overdrive variations, as described in Sec. 2. At elevated temperatures, future nanometer CMOS circuits will operate faster, thereby producing significant timing slack in the constant clock period.

The amount of heat dissipated by an integrated circuit is dependent on the switching activity and the power consumption.[4] Die temperature is further determined by the variations in the ambient temperature where a circuit is deployed. Higher die temperature exponentially increases the leakage currents.[4] Increased leakage power, inturn, further enhances the heat dissipation and elevates the

die temperature. This positive feedback between the die temperature, the leakage current, and the total power consumption accelerates the degradation of the device/circuit reliability due to excessive heating and can cause thermal runaway. New temperature-adaptive design methodologies are, therefore, highly desirable to enhance the reliability and the energy efficiency of deeply scaled nanometer CMOS circuits.

In this paper, temperature-adaptive supply and threshold voltage tuning techniques are proposed to dynamically adjust the circuit speed based on the die temperature, as illustrated in Fig. 5. The primary objective of the proposed temperature-adaptive schemes is to lower the active-mode energy consumption by exploiting the excessive timing slack produced in the clock period at high die temperatures while maintaining a constant-clock frequency across an entire die temperature spectrum. The objective is achieved by either dynamically scaling the power supply voltage or dynamically increasing the device threshold voltages through reverse body-bias at elevated temperatures.

### 3.1. *Temperature-adaptive dynamic supply voltage scaling*

The temperature-adaptive dynamic supply voltage tuning technique is presented in this section. Both dynamic switching and leakage energy consumption are more than quadratically reduced by scaling the supply voltage of a circuit. The propagation

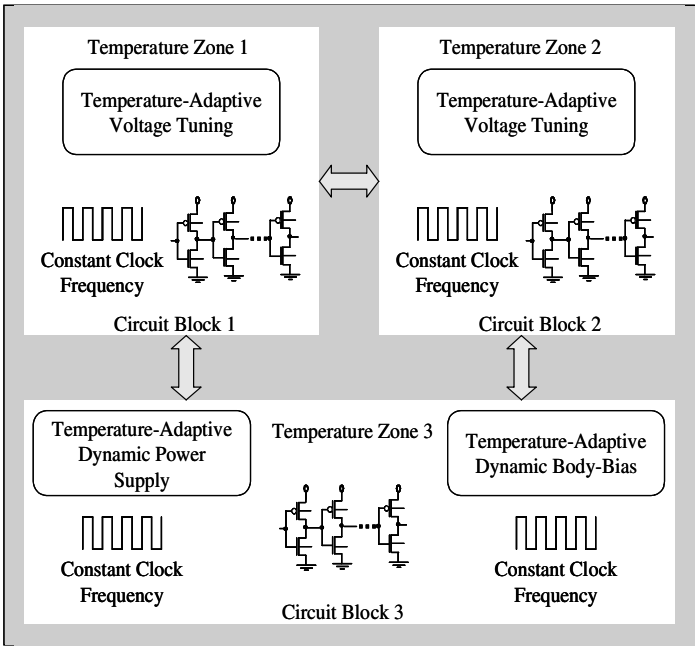


Fig. 5. An integrated circuit with multiple temperature zones. The local supply voltage or the threshold voltages are dynamically scaled to lower the energy consumption while maintaining a constant clock frequency across the die.

delay of a circuit is also strongly dependent on the supply voltage.[4] Scaling the supply voltage reduces the energy consumed by a circuit at the cost of degraded circuit performance.

In nanometer CMOS circuits that exhibit reversed temperature dependence, the supply voltage of a circuit can be dynamically scaled at elevated temperatures without degrading the clock frequency. The supply voltage can be tuned until the high temperature circuit performance at the scaled supply voltage matches the circuit performance at the nominal voltages and the lowest operating temperature. Unlike the conventional work-load adaptive dynamic voltage scaling techniques,[4–6] a new die-temperature-adaptive dynamic voltage scaling technique is proposed in this paper for tuning the circuit supply voltage based on the fluctuations of the die temperature and the circuit speed.

An integrated circuit with multiple temperature zones is shown in Fig. 5. Imbalanced utilization and diversity of circuitry within an integrated circuit (IC) leads to higher heat dissipation in certain areas of the die, thereby producing local hotspots.[1] During the design process, the integrated circuit is simulated under typical workload conditions to obtain the temperature profile of the die. Based on the die temperature profile, an IC can be partitioned into multiple temperature domains, as shown in Fig. 5. The power supply in each temperature zone can be dynamically tuned for lower energy consumption while maintaining a constant clock frequency across the die. Alternatively, in an IC with a uniform die temperature, the supply voltage of the entire circuit can be dynamically tuned based on the changes in the ambient temperature for achieving enhanced energy efficiency while maintaining a constant clock frequency.

The temperature-adaptive supply voltage tuning is illustrated in Fig. 6. The target operating frequency ($f_{\text{target}}$) of an integrated circuit is determined for the nominal supply voltage at the lowest operating temperature. A ring oscillator providing

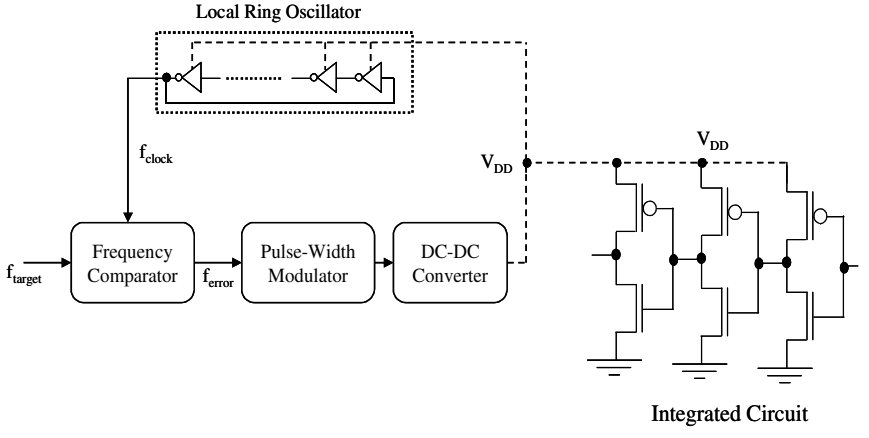


Fig. 6. Temperature-adaptive dynamic supply voltage scaling technique.

a replica of the critical path of the circuitry in a temperature zone (or the critical path of the entire IC in case of a uniform die temperature) is employed to track the fluctuations of the clock frequency with the variations of the die temperature at a specific supply voltage. The ring oscillator translates the variations in the die temperature to a specific clock frequency ($f_{\text{clock}}$) for a specific power supply voltage generated by the DC–DC converter. As the die temperature increases, the ring oscillator frequency ($f_{\text{clock}}$) also increases due to the enhanced gate overdrive voltages of the MOSFETs. The ring oscillator frequency is compared to the target clock frequency ($f_{\text{target}}$), generating a frequency error signal ($f_{\text{error}}$). The pulse width modulator using this error signal generates the control signals for the DC–DC converter to either modify or maintain the output voltage. The power supply voltage is, thereby, dynamically tuned based on the variations of the die temperature using the closed loop feedback circuitry shown in Fig. 6.

The normalized high temperature propagation delay of circuits at different scaled supply voltages along with the propagation delay at the room temperature (25°C) and the nominal supply voltage ($V_{\text{DD}} = 0.7\,\text{V}$) is shown in Fig. 7. The appropriate amount of voltage scaling for maintaining the clock frequency is bordered with a demarcation line in Fig. 7. The scaled optimum supply voltages ($V_{\text{DD,opt}}$) that maintain the circuit speed at high temperatures are 10% (carry select adder and Brent–Kung adder) to 11.4% (array multiplier) lower than the nominal supply voltage in this technology, as shown in Fig. 7. The normalized high temperature energy consumption at the optimum and the nominal supply voltages are shown in Fig. 8. As shown in Fig. 8, the high temperature energy consumption is reduced by 19.1% (carry select adder and Brent–Kung adder) to 21% (array multiplier) with the temperature-adaptive dynamic supply voltage scaling technique as compared to the standard circuit operation at the nominal voltages.

An important source of noise in CMOS integrated circuits is the power supply noise.[4] The impact of supply voltage variations on the effectiveness of the proposed

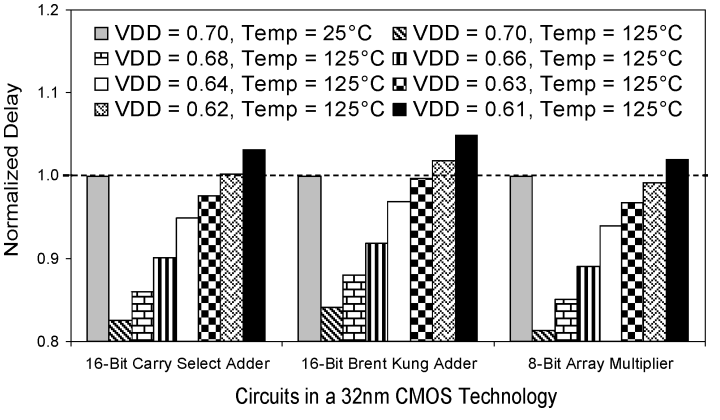


Fig. 7. Normalized propagation delay of circuits at different supply voltages and temperature.

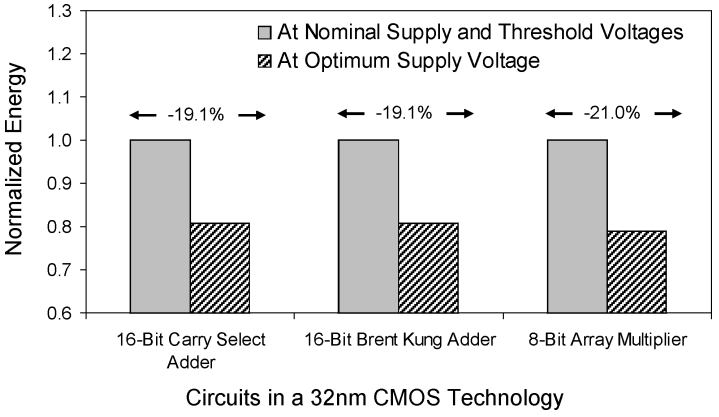


Fig. 8. Normalized high temperature (125°C) energy consumption at the nominal and optimum supply voltages.

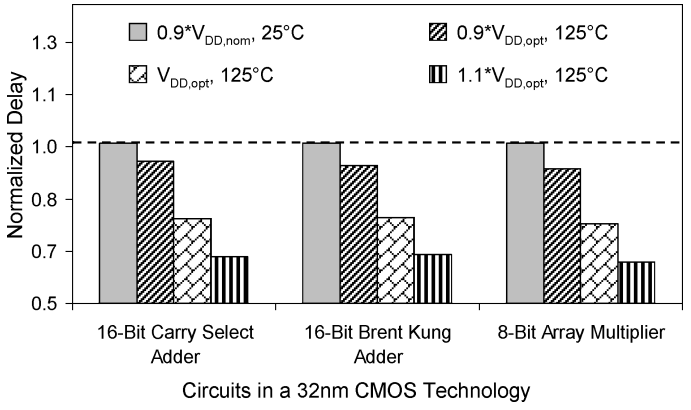


Fig. 9. Normalized propagation delay of circuits with the nominal and optimum supply voltages under the impact of power supply noise.

temperature-adaptive dynamic supply voltage scaling technique is also evaluated in this paper. Integrated circuits are typically designed to meet the performance specifications at a voltage 10% lower than the nominal supply voltage to account for the supply voltage variations.[4] The maximum fluctuation of the supply voltage is therefore assumed to be $\pm 10\%$ in this paper. The propagation delays of the circuits under the impact of worst-case supply voltage variations are shown in Fig. 9. The worst-case circuit speed at the degraded optimum supply voltages ($0.9{*}V_{\mathrm{DD,opt}}$) are higher than the worst-case speed of the nominal $V_{\mathrm{DD}}$ circuits subject to the maximum supply voltage variation ($0.9{*}V_{\mathrm{DD,nom}}$), as shown in Fig. 9. Circuits with guaranteed functionality for the worst-case fluctuation of the nominal supply voltage are therefore also guaranteed to satisfy the performance requirements for the worst-case degradation of the optimum supply voltage. The impact of the power supply noise on the performance and the functionality of the temperature-adaptive

voltage tuning circuits is therefore a lesser concern as compared to the standard nominal voltage circuitry.

### 3.2. *Temperature-adaptive body-bias*

The temperature-adaptive threshold voltage tuning technique is presented in this section. Similar to the dependence on the supply voltage, the propagation delay of a circuit is also strongly dependent on the device threshold voltages.[4] The absolute value of the threshold voltages degrade as the temperature increases, thereby simultaneously enhancing the circuit speed and the subthreshold leakage currents at elevated temperatures.[4,14] In scaled nanometer CMOS circuits that exhibit reversed temperature dependence, the threshold voltages of devices can be increased at elevated temperatures to reduce the leakage current without degrading the clock frequency. The device threshold voltages can be dynamically increased until the high temperature circuit performance matches the circuit performance with the standard zero body-bias threshold voltages at the lowest operating temperature.

The threshold voltage can be dynamically increased by reverse body-bias.[4] Applying reverse body-bias reduces the subthreshold leakage current while increasing the junction leakage due to enhanced band-to-band tunneling. For small body-bias voltages, the reduction in the subthreshold leakage can be substantially higher as compared to the increase in the band-to-band tunneling current, as described in Ref. 4. The source and drain-to-body junction capacitances of reverse body-biased devices are also reduced, thereby further enhancing the active mode energy efficiency as compared to a standard zero body-biased circuit. Unlike the conventional body-bias techniques aimed at altering the device threshold voltages based on the variations of the workload and the circuit activity,[4,7–11] a new temperature-adaptive body-bias technique is proposed in this paper for altering the threshold voltages of the devices based on the fluctuations of the die temperature and the circuit speed. Similar to the temperature-adaptive dynamic supply voltage tuning technique, the threshold voltages of the devices in individual temperature zones (or the entire IC provided that the die temperature is uniform) can be dynamically tuned based on the fluctuations of the die temperature with the goal of maintaining constant propagation delays across the temperature spectrum.

The temperature-adaptive body-bias technique is illustrated in Fig. 10. A ring oscillator providing a replica of the critical path of the circuitry in a temperature zone (or the critical path of the entire IC for a uniform die temperature) is employed to track the variations of the clock frequency with the die temperature for a set of body-bias voltages. The ring oscillator translates the (local) die temperature to a specific clock frequency ($f_{\text{clock}}$) for a specific set of body-bias voltages produced by the PMOS and NMOS body-bias generators. The ring oscillator frequency ($f_{\text{clock}}$) is compared with the target operating frequency ($f_{\text{target}}$) of the integrated circuit and a frequency error signal ($f_{\text{error}}$) is generated. Using this error signal, the body-bias

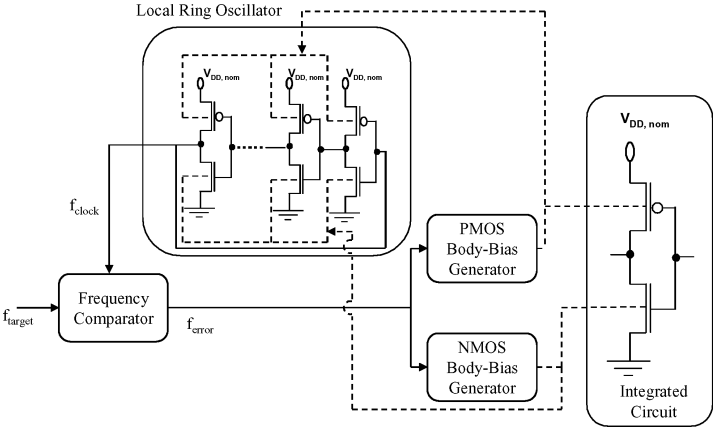


Fig. 10. Temperature-adaptive body-bias technique. $V_{\mathrm{DD,nom}}$: the nominal supply voltage.

generators either modify or maintain the body-bias voltages applied to the devices in the integrated circuit. The device threshold voltages are, thereby, dynamically tuned based on the die temperature variations using the feedback circuitry shown in Fig. 10.

The temperature-adaptive body-bias technique is applied to three test circuits. All the devices in the circuits are dynamically reverse body-biased to suppress the active mode leakage current at elevated temperatures. The normalized high temperature propagation delay at different body-bias voltages along with the propagation delay of the standard zero body-biased circuits at the room temperature (25°C) is shown in Fig. 11. The optimum reverse body-bias (RBB) voltages required to maintain the circuit speed at elevated temperatures are from 0.12 V (Brent–Kung adder) to 0.14 V (carry select adder and array multiplier), as shown in Fig. 11.

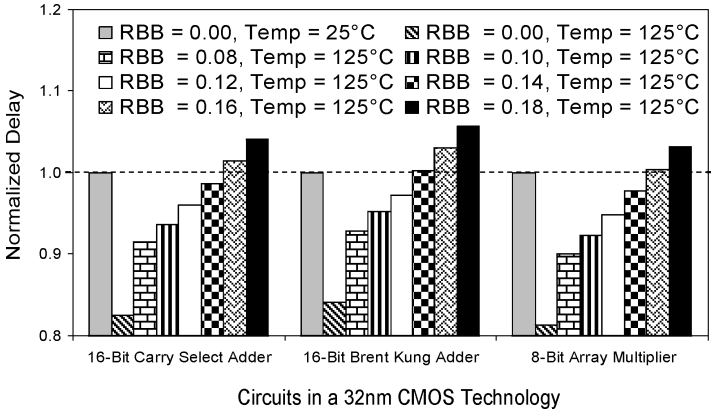


Fig. 11. Normalized propagation delay for different body-bias voltages and temperature. RBB is the absolute value of the reverse body-bias voltage $|V_{\mathrm{SB}}|$ applied to all the devices in the circuits.

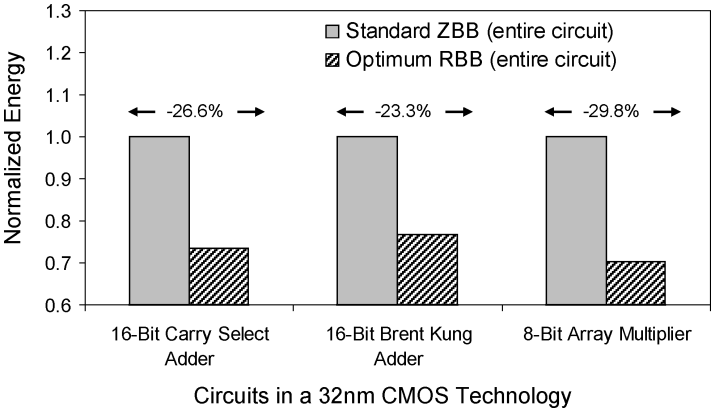


Fig. 12. Normalized high temperature (125°C) active mode energy consumed by the standard zero body-biased (ZBB) and the optimum reverse body-biased (RBB) circuits.

The high temperature active mode energy consumption of the reverse body-biased circuits are compared to the standard zero body-biased circuits in Fig. 12. The energy consumed at the optimum body-bias voltages are normalized to the energy consumed by the corresponding zero body-biased circuit at 125°C. As shown in Fig. 12, the high temperature active mode energy consumption is reduced by 23.3% (Brent–Kung adder) to 29.8% (array multiplier) with the temperature-adaptive body-bias technique as compared to the standard zero body-biased circuits.

## 4. High Temperature Energy Reduction with the Temperature-Adaptive Schemes

The tradeoffs in the implementation of the temperature-adaptive voltage tuning schemes are presented in this section. A comparison of the percent energy reduction provided with the two temperature-adaptive schemes is shown in Fig. 13. The high temperature energy savings offered with the temperature-adaptive reverse body-bias technique is up to 1.4× higher as compared to the temperature-adaptive dynamic supply voltage tuning technique, as shown in Fig. 13. Static energy consumption due to leakage currents is expected to exceed the dynamic switching energy in the near future.[4,16] Increasing the device threshold voltages through reverse body-bias reduces the leakage currents as well as the device junction parasitic capacitances. The temperature-adaptive reverse body-bias technique is therefore very effective to lower the energy consumed by the active CMOS circuits at high temperatures, as shown in Fig. 13. The effectiveness of the technique would be further enhanced if the lowest die temperature is less than 25°C due to the active cooling (refrigeration) or the deployment of a circuit at very low ambient temperatures.

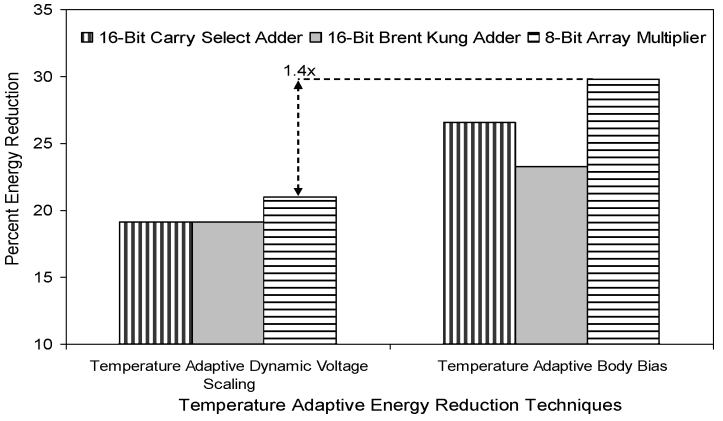


Fig. 13. Comparison of the percent energy reduction provided with the proposed temperature-adaptive schemes.

The proposed temperature-adaptive schemes can be implemented in a standard n-well or p-well CMOS technology. The temperature-adaptive energy reduction schemes require an energy efficient high resolution voltage scaling power supply because of the low nominal and optimum supply and body-bias voltages associated with the deeply-scaled nanometer CMOS circuits. The energy overheads related with modifying the voltage of the high parasitic capacitance of the substrate (or the wells) and the power distribution network and with generating the different body-bias and power supply voltages should be further investigated to evaluate the net energy reduction provided with the proposed temperature-adaptive techniques. The impact of inter-die and intra-die process parameter variations is assumed to be small in this paper. The effectiveness of the proposed temperature adaptive voltage tuning schemes under process parameter variations will be investigated in the future.

The variation of the temperature of a die is typically a slow process as presented in Ref. 17. Because of the gradual fluctuations of the die temperature over time and a wide range of ambient temperatures experienced depending on the circuit activity and where the circuit is deployed, a finer-temperature-grain supply or threshold voltage tuning technique can be employed. The adaptation of the circuit speed to the intermediate die temperatures through dynamic voltage tuning would further enhance the energy savings provided with the proposed techniques.

It should also be noted that the proposed temperature-adaptive voltage scaling technique is applicable without degrading the clock frequency only in circuits that display reversed temperature dependence where the circuit speed is enhanced with increased temperature. The supply voltage of a circuit in an older CMOS technology generation where the performance degrades at elevated temperatures cannot be scaled without degrading the clock frequency.

## 5. Conclusions

Gate overdrive variation with temperature dominates the speed characteristics of deeply scaled CMOS circuits. The propagation delay is reduced with the increased temperature in a 32 nm CMOS technology, indicating a complete reversal in the temperature dependent speed characteristics of nanometer CMOS circuits. The reversal in the temperature dependent speed characteristics provides new opportunities to lower the active mode energy consumption at high temperatures. Temperature-adaptive dynamic supply and threshold voltage tuning techniques are proposed in this paper to reduce the high temperature energy consumption without degrading the clock frequency in active CMOS circuits.

The temperature-adaptive voltage scaling technique dynamically adjusts the power supply voltage of a circuit based on the die-temperature fluctuations. The high temperature energy consumed with the temperature-adaptive voltage scaling technique is 19.1%–21% lower as compared to the energy consumed at the nominal voltages. Alternatively, the temperature-adaptive body-bias technique dynamically tunes the threshold voltages of the devices based on the fluctuations of the die temperature and the circuit speed. The high temperature active mode energy is reduced by up to 29.8% with the temperature-adaptive reverse body-bias technique as compared to the standard zero body-biased circuits. Dynamically increasing the threshold voltages of the devices through temperature-adaptive reverse body-bias is shown to be very effective to reduce the high temperature energy consumption while maintaining constant speed in the active mode in deeply scaled nanometer CMOS integrated circuits.

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