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Voltage optimization for simultaneous energy efficiency and temperature variation resilience in CMOS circuits ☆

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Abstract

A design technique based on optimizing the supply voltage for simultaneously achieving energy efficiency and temperature variation insensitive circuit performance is proposed in this paper. The supply voltages that suppress the propagation delay variations when the temperature fluctuates are identified for a diverse set of circuits in 180 and 65 nm CMOS technologies. Circuits display temperature variation insensitive propagation delay when operated at a supply voltage 44–47% lower than the nominal supply voltage ($V_{DD} = 1.8$ V) in a 180 nm CMOS technology. Similarly, the optimum supply voltages are 67–68% lower than the nominal supply voltage ($V_{DD} = 1.0$ V) in a 65 nm CMOS technology. At scaled supply voltages, integrated circuits consume lower power at the cost of reduced speed. The proposed design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance is, therefore, particularly attractive for low-power applications with relaxed speed requirements. A new design methodology based on threshold voltage optimization for achieving temperature variation insensitive circuit speed is also evaluated. The energy per cycle and the propagation delay at the supply and threshold voltages providing temperature variation insensitive circuit performance, minimum energy-delay product, and minimum energy are compared. Results indicate that low-power operation and temperature variation tolerance can be simultaneously achieved with the proposed techniques.

Keywords: Minimum energy; Minimum energy-delay product; Propagation delay fluctuations; Supply voltage optimization; Temperature variations; Threshold voltage optimization

1. Introduction

Process and environment parameter variations in scaled CMOS technologies are posing greater challenges in the design of reliable integrated circuits. Because of the unbalanced utilization and diversity of circuitry at different sections of an integrated circuit, temperature can vary significantly from one die area to another [1]. Furthermore, environmental temperature fluctuations can cause significant variations in die temperature. For example, electronic systems mounted on automobile engines operate at a temperature range from −40 to 150 °C [2,3]. Temperature variations affect the device characteristics of MOSFETs thereby varying the performance of integrated circuits.

The supply and threshold voltages are scaled with each new technology generation. The supply voltage is scaled primarily based on the device reliability and target clock frequency requirements in a new technology generation. Scaling the device dimensions strengthens the electric fields between device terminals while lowering the parasitic capacitances, thereby increasing the speed of CMOS integrated circuits. The speed of a circuit can be further enhanced by scaling the threshold voltages. Due to the subthreshold leakage current constraints, however, the threshold voltages are scaled at a much slower rate as compared to the supply voltage. The supply voltage to threshold voltage ratio is reduced with each new technology generation. The temperature fluctuation induced threshold voltage variation is therefore expected to have an increasingly important role in determining the

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MOSFET drain current variations when the temperature fluctuates. A complete reversal of temperature dependent speed characteristics of CMOS circuits is also likely to occur in the near future [4].

Propagation delay of a circuit is a function of the drain saturation current produced by active transistors. Temperature fluctuations alter threshold voltage, carrier mobility, and saturation velocity of a MOSFET [5,22]. Temperature fluctuation induced variations in individual device parameters have unique effects on MOSFET drain current. Performance variation of an integrated circuit under temperature fluctuations is determined by the device parameter whose variation dominates the drain current produced by the MOSFETs.

Temperature dependent device parameters that cause MOSFET drain current variations in the TSMC 180 nm and the predictive 65 nm CMOS technologies are identified in this paper. A design methodology based on optimizing the supply voltage for temperature variation insensitive circuit performance is proposed. The optimum supply voltages that achieve temperature variation insensitive propagation delay for a diverse set of circuits in 180 and 65 nm CMOS technologies are presented.

In circuits that exhibit reversed temperature dependence, the optimum supply voltages that yield temperature variation insensitive delay are higher than the nominal supply voltage [4]. Alternatively, the optimum supply voltages are lower than the nominal supply voltage in 180 and 65 nm CMOS technologies. Integrated circuits operating at scaled supply voltages consume low power at the cost of reduced speed. The design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance in 180 and 65 nm CMOS technologies is, therefore, particularly attractive in low-power applications with relaxed speed requirements.

In this paper, the supply voltages that achieve minimum energy-delay product and minimum energy are identified at two different temperatures for circuits in the TSMC 180 nm and the predictive 65 nm CMOS technologies. The energy per cycle and speed at the supply voltages providing temperature variation insensitive propagation delay, minimum energy-delay product, and minimum energy are compared. An alternative method based on threshold voltage optimization for suppressing the propagation delay variations when the temperature fluctuates is also evaluated. The speed and energy tradeoffs with the two optimization techniques are compared.

The paper is organized as follows. The influence of temperature dependent device parameters on the drain current of a MOSFET is analyzed in Section 2. Effect of temperature fluctuations on the device and circuit characteristics is examined in Section 3. The optimum supply voltages providing temperature variation insensitive circuit performance are presented in Section 4. The supply voltages that yield minimum energy-delay product and minimum energy are identified in Section 5. The tradeoffs of operating the circuits at the supply voltages providing temperature variation insensitive circuit speed are discussed in Section 6. The threshold voltage optimization technique for temperature variation insensitive speed is presented in Section 7. Finally, some conclusions are given in Section 8.

2. Factors influencing MOSFET current under temperature fluctuations

Device parameters that are affected by temperature fluctuations, causing variations in the drain current produced by a MOSFET, are identified in this section. BSIM3 and BSIM4 MOSFET current equations are used for an accurate characterization of temperature fluctuation induced drain current variations in deeply scaled nanometer devices. The drain current of a MOSFET is [6–8]

$$I_{ds} \propto \frac{I_{ds0}}{1 + R_{ds} I_{ds0} / V_{dseff}}, \tag{1}$$

$$I_{ds0} \propto \frac{V_{gsteff} \mu_{eff} V_{dseff} (1 - A_{bulk} V_{dseff} / 2(V_{gsteff} + 2V_T))}{(1 + V_{dseff} / E_{SAT} L_{eff})}, \tag{2}$$

where I_{ds}, I_{ds0}, R_{ds}, V_{dseff}, V_{gsteff}, A_{bulk}, μ_{eff}, V_T, E_{SAT}, and L_{eff} are the drain current with short-channel effects, drain current of a long channel device, parasitic drain-to-source resistance, effective drain-to-source voltage, effective gate overdrive ($V_{GS} - V_t$), parameter to model the bulk charge effect, effective carrier mobility, thermal voltage, electric field at which the carrier drift velocity saturates, and effective channel length, respectively.

Threshold voltage, saturation velocity, and carrier mobility are [7,8]

$$\text{NMOS}: V_t(T) = V_t(T_0) + \left(KT1 + \frac{KT1L}{L_{eff}} + V_{bseff} KT2\right) \times \left(\frac{T}{T_0} - 1\right), \tag{3}$$

$$\text{PMOS}: V_t(T) = V_t(T_0) - \left(KT1 + \frac{KT1L}{L_{eff}} + V_{bseff} KT2\right) \times \left(\frac{T}{T_0} - 1\right), \tag{4}$$

$$V_{SAT}(T) = V_{SAT}(T_0) - AT\left(\frac{T}{T_0} - 1\right), \tag{5}$$

$$\mu_{eff}(T) = \left(U_0 \left(\frac{T}{T_0}\right)^{U_{te}}\right) \left\{1 + \left(\frac{V_{gsteff} + 2V_t(T)}{T_{OXE}}\right)^2 U_b(T) + (U_c(T) V_{bseff} + U_a(T)) \left(\frac{V_{gsteff} + 2V_t(T)}{T_{OXE}}\right)\right\}^{-1}, \tag{6}$$

where V_t, $KT1$, $KT1L$, $KT2$, V_{bseff}, U_0, U_{te}, T_{OXE}, U_a, U_b, U_c, V_{SAT}, AT, T_0, and T are the threshold voltage with short-channel effects, temperature coefficient for threshold voltage, channel length dependence of the temperature

coefficient for threshold voltage, body-bias coefficient of threshold voltage temperature effect, effective substrate bias voltage, mobility at the reference temperature, mobility temperature exponent, electrical gate-oxide thickness, first order mobility degradation coefficient, second order mobility degradation coefficient, body effect of mobility degradation coefficient, saturation velocity, temperature coefficient of saturation velocity, reference temperature, and the operating temperature, respectively. *KT1*, *KT1L*, *KT2*, and *AT* are constant empirical parameters while U_a, U_b, and U_c are temperature dependent [7,8]. U_a, U_b, and U_c are

$$U_a(T) = U_a(T_0) + U_{a1}\left(\frac{T}{T_0} - 1\right), \tag{7}$$

$$U_b(T) = U_b(T_0) + U_{b1}\left(\frac{T}{T_0} - 1\right), \tag{8}$$

$$U_c(T) = U_c(T_0) + U_{c1}\left(\frac{T}{T_0} - 1\right), \tag{9}$$

where U_{a1}, U_{b1}, and U_{c1} are the temperature coefficients of U_a, U_b, and U_c, respectively. As given by (3), (4), (5), and (6), absolute values of threshold voltage, carrier mobility, and saturation velocity degrade as the temperature is increased [7,8,22]. The saturation velocity is typically a weak function of temperature [5]. Threshold voltage degradation with temperature tends to enhance the drain current because of the increase in gate overdrive ($V_{GS} - V_t$). Alternatively, degradation in carrier mobility tends to lower the drain current as given by (1) and (2). Effective variation of MOSFET current is, therefore, determined by the variation of the dominant device parameter when the temperature fluctuates.

3. Device and circuit behavior under temperature fluctuations

Influence of temperature fluctuations on the device and circuit characteristics in the TSMC 180 nm [9] and the predictive 65 nm CMOS [10] technologies are evaluated in this section. The model parameter coefficients that determine the temperature fluctuation induced MOSFET drain current variations are listed in Table 1. Temperature fluctuation induced gate overdrive and carrier mobility variations at the nominal supply voltage are shown in Figs. 1 and 2 for devices in 180 and 65 nm CMOS technologies, respectively. The nominal supply voltages are 1.8 and 1.0 V for the 180 and 65 nm CMOS technologies, respectively. The device threshold voltages excluding the short-channel effects ($|V_{t0}|$) are 0.46 and 0.22 V for the 180 and 65 nm CMOS technologies, respectively. Variation of the drain current (I_{DS}) of transistors in 180 and 65 nm CMOS technologies with the temperature is shown in Figs. 3 and 4, respectively.

Table 1
Model coefficients that effect the MOSFET drain current when the temperature fluctuates

Model parameters	180 nm CMOS technology		65 nm CMOS technology	
	PMOS	NMOS	PMOS	NMOS
*KT*1	−0.214	−0.196	−0.110	−0.110
*KT*1*L*	0	0	0	0
*KT*2	−0.035	−0.039	0.022	0.022
U_{te}	−0.599	−1.945	−1.500	−1.500
U_{a1}	1.22E−09	1.22E−09	4.31E−09	4.31E−09
U_{b1}	−1.44E−18	−3.08E−18	7.61E−18	7.61E−18
U_{c1}	1.97E−10	−2.39E−10	−5.60E−11	−5.60E−11
AT	10 000	20 000	33 000	33 000

At the nominal supply voltage, variations of the gate overdrive are smaller as compared to the carrier mobility variations when the temperature is increased from 25 to 125 °C. The drain current of devices operating at the nominal supply voltage is, therefore, degraded as shown in Figs. 3 and 4. Test circuits are designed to have equal low-to-high and high-to-low propagation delays at the nominal supply voltage and 125 °C. Propagation delay variations with temperature for circuits operating at the nominal supply voltage in 180 and 65 nm CMOS technologies are shown in Figs. 5 and 6, respectively. The circuit speed at the nominal supply voltage degrades primarily due to the reduction of MOSFET currents following the degradation

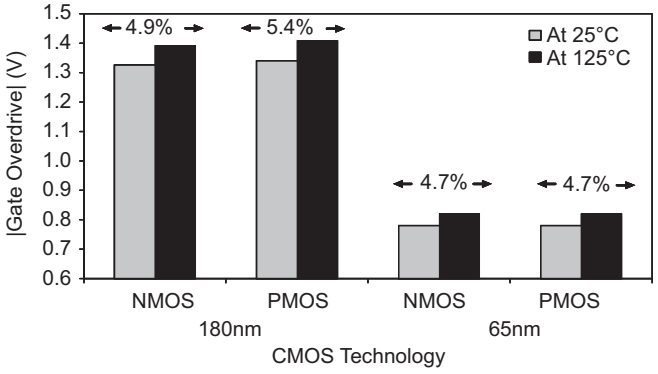

Fig. 1. Gate overdrive variation with temperature at the nominal supply voltage.

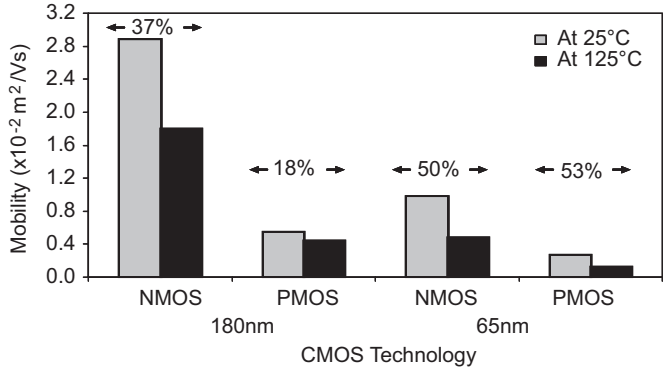

Fig. 2. Mobility variation with temperature at the nominal supply voltage.

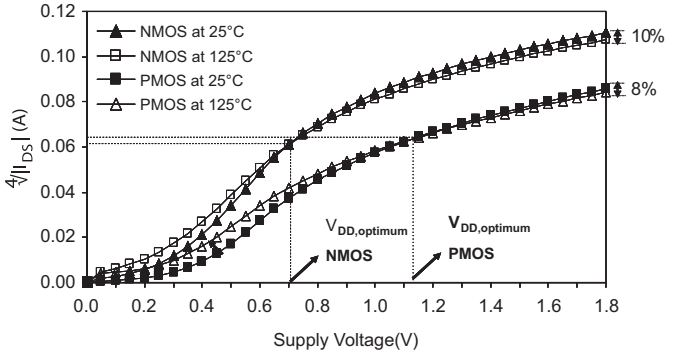

Fig. 3. Variation of MOSFET drain current with supply voltage and temperature in the TSMC 180 nm CMOS technology. $|V_{DS}| = |V_{GS}| = V_{DD}$ and $|V_{t0}(T_0)| = 0.46$ V.

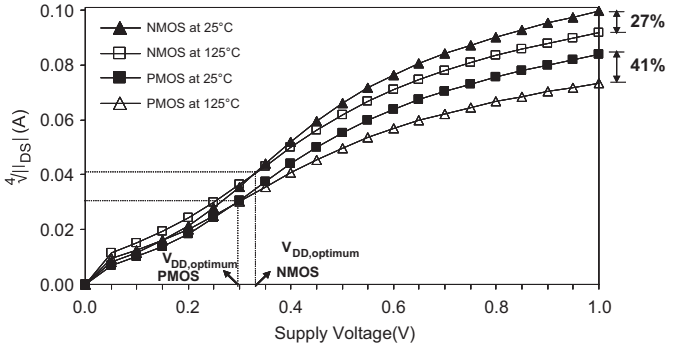

Fig. 4. Variation of MOSFET drain current with supply voltage and temperature in the predictive 65 nm CMOS technology. $|V_{DS}| = |V_{GS}| = V_{DD}$ and $|V_{t0}(T_0)| = 0.22$ V.

of carrier mobilities when the temperature is increased. When operating at the nominal supply voltage, the speed of circuits degrades by up to 15.9% and 54.5% as the temperature is increased from 25 to 125 °C in 180 and 65 nm CMOS technologies, respectively.

4. Supply voltage optimization for temperature variation insensitive delay

The results presented in Section 3 indicate that operating an integrated circuit at the prescribed nominal supply voltage is not preferable for reliable circuit operation under temperature fluctuations. A design methodology based on scaling the supply voltage for suppressing the drain current variations due to temperature fluctuations is described in [4,11–13]. In order to compensate for the variation of carrier mobility, the sensitivity of gate overdrive to temperature fluctuations should be enhanced by lowering the supply voltage. At the optimum supply voltage, the temperature fluctuation induced gate overdrive variation completely counterbalances the carrier mobility variation. A transistor biased at this optimum supply voltage produces a temperature variation insensitive constant drain current, as illustrated in Figs. 3 and 4.

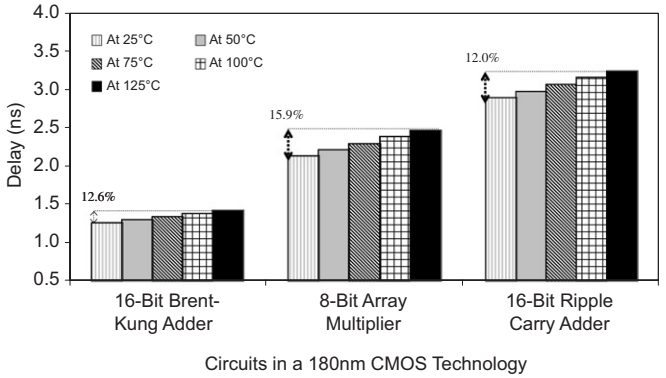

Fig. 5. Percent delay variation with temperature for circuits operating at the nominal supply voltage ($V_{DD} = 1.8$ V) in the TSMC 180 nm CMOS technology.

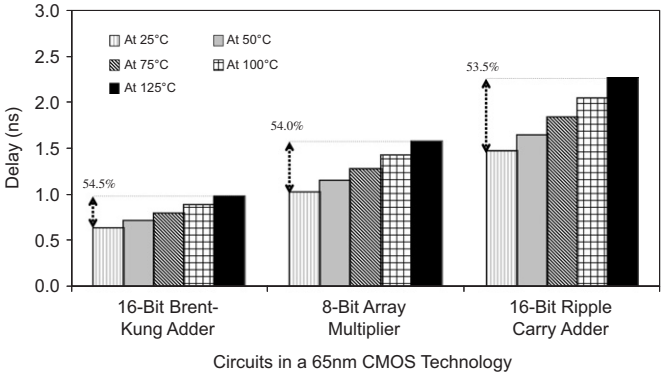

Fig. 6. Percent delay variation with temperature for circuits operating at the nominal supply voltage ($V_{DD} = 1.0$ V) in the predictive 65 nm CMOS technology.

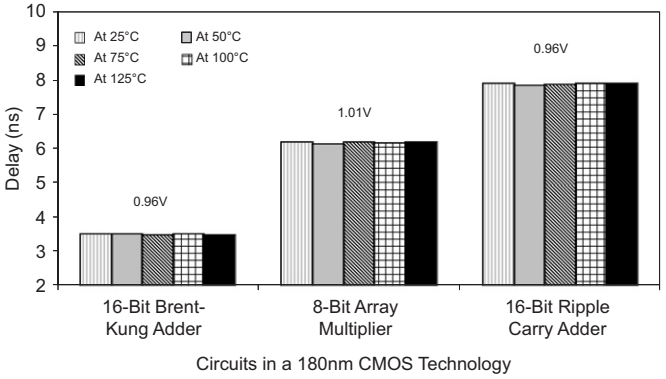

Fig. 7. Optimum supply voltages that achieve temperature variation insensitive speed characteristics in the TSMC 180 nm CMOS technology.

The optimum supply voltages for circuits in 180 and 65 nm CMOS technologies are shown in Figs. 7 and 8, respectively. Circuits display a temperature variation insensitive behavior when operated at a supply voltage 44–47% lower than the nominal supply voltage in a 180 nm CMOS technology. Similarly, the optimum supply voltages

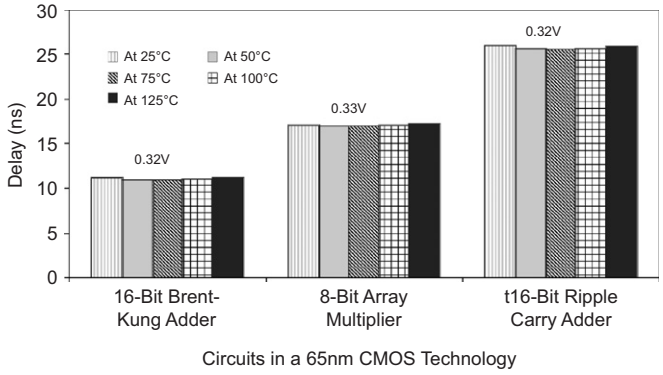

Fig. 8. Optimum supply voltages that achieve temperature variation insensitive speed characteristics in the predictive 65 nm CMOS technology.

are 67–68% lower than the nominal supply voltage for circuits in a 65 nm CMOS technology. The optimum supply voltages are similar for a diverse set of circuits in both technologies. The proposed technique of operating large scale designs at an optimum supply voltage for diminishing the performance sensitivity to temperature fluctuations is, therefore, feasible.

5. Supply voltages for minimum energy-delay product and minimum energy

The results presented in Section 4 indicate that there is an optimum supply voltage at which the speed characteristics of an integrated circuit are insensitive to temperature fluctuations. The supply voltage that achieves temperature variation insensitive circuit performance is lower than the nominal supply voltage. Integrated circuits operating at scaled supply voltages consume lower power at the cost of reduced speed. The design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance is, therefore, particularly attractive in low-power applications with relaxed speed requirements.

Low-power designs are typically aimed at reducing either power, or power-delay product, or energy-delay product [14–17]. Energy-delay product metric provides a good compromise between the need to reduce the energy consumption and the requirement to operate the circuits at an appropriate speed [14]. The energy-delay product is [14,17,18]

$$\mathrm{EDP} \approx \sum_j C_{\mathrm{eff},j} V_{\mathrm{DD}}^2 T_{\mathrm{g}} + \sum_j \sum_{j_i} I_{\mathrm{leak},j_i} V_{\mathrm{DD}} T_{\mathrm{g}} T_{\mathrm{c}}, \quad (10)$$

$$I_{\mathrm{leak},j_i} = \frac{\mu_{j_i} W_{j_i} C_{\mathrm{OX}}}{L_{\mathrm{eff}}} V_{\mathrm{T}j_i}^2 \mathrm{e}^{(|V_{\mathrm{GS}j_i}|-|V_{\mathrm{t},j_i}|)/n_{j_i} V_{\mathrm{T}j_i}} \times (1-\mathrm{e}^{-|V_{\mathrm{DS}j_i}|/V_{\mathrm{T}j_i}}), \quad (11)$$

where EDP, I_{leak}, V_{DD}, T_{g}, T_{c}, μ, W, C_{OX}, L_{eff}, V_{t}, V_{T}, V_{GS}, V_{DS}, and n are energy-delay product, subthreshold leakage current, supply voltage, propagation delay of the circuit, clock period, carrier mobility, transistor width, oxide capacitance per unit area, effective channel length, threshold voltage with short-channel effects, thermal voltage, gate-to-source voltage, drain-to-source voltage, and subthreshold swing coefficient, respectively. C_{eff} is the average effective switching capacitance of each gate that is extracted to include the average activity factor and the energy consumed due to short circuit current and glitches. The indices j and i cover all of the gates in the circuit and all of the transistors that determine the net subthreshold leakage current of each gate, respectively.

The normalized energy per cycle, delay, and energy-delay product as a function of the supply voltage at the room temperature (25 °C) for an inverter in a 180 nm CMOS technology is shown in Fig. 9. As the supply voltage is reduced, the energy per cycle decreases while the propagation delay increases [14–17]. The energy-delay product given by (10), therefore, has a minimum, as shown in Fig. 9.

Energy per cycle and propagation delay are also dependent on the die temperature [13–16]. As the temperature increases, energy consumed by a circuit increases primarily due to the increase in subthreshold leakage current [18]. Similarly, the propagation delay of circuits in current CMOS technologies increase when the temperature is increased at the nominal supply voltage, primarily due to the degradation in carrier mobility as explained in Sections 2 and 3. Circuits that operate with the nominal supply voltage, therefore, display the worst case energy-delay product at the maximum temperature for which the circuit is functional.

Speed characteristics of circuits are also dependent on the supply voltage [4]. The temperature fluctuation induced gate overdrive and carrier mobility variations at different supply voltages for devices in a 180 nm CMOS technology are presented in Table 2. As listed in Table 2, scaling the supply voltage enhances the sensitivity of gate-overdrive to temperature variations. At supply voltages below the optimum supply voltage, the gate overdrive variations dominate the carrier mobility variations when the temperature fluctuates. The MOSFET drain current and the

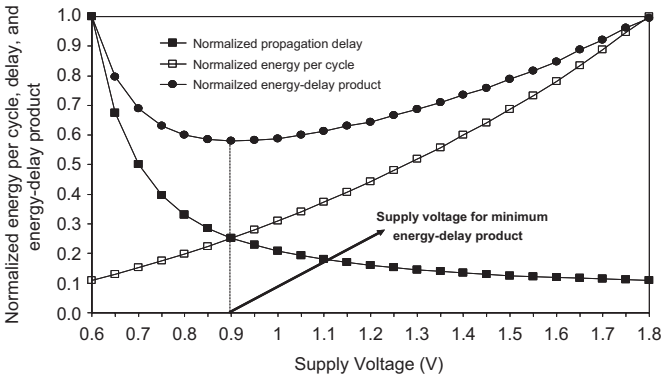

Fig. 9. Normalized energy per cycle, delay, and energy-delay product as a function of the supply voltage at the room temperature (25 °C) for an inverter in the TSMC 180 nm CMOS technology.

Table 2
Gate overdrive and carrier mobility variations at different supply voltages for devices in a 180 nm CMOS technology

Supply voltage (V)	Temperature (°C)	Gate overdrive (V)		Carrier mobility ($\times 10^{-3}$ m^2/Vs)	
		PMOS	NMOS	PMOS	NMOS
1.8	25	−1.34	1.33	5.46	28.86
	125	−1.41	1.39	4.47	17.93
	Variation (%)	5.37	4.95	−18.26	−37.87
1.1	25	−0.64	0.63	6.31	35.10
	125	−0.71	0.69	5.13	20.08
	Variation (%)	11.28	10.48	−18.69	−42.78
0.7	25	−0.24	0.23	6.98	37.78
	125	−0.31	0.29	5.70	20.95
	Variation (%)	30.39	29.01	−18.36	−44.54
0.5	25	−0.04	0.03	7.39	38.66
	125	−0.11	0.09	6.06	21.25
	Variation (%)	198.88	249.31	−17.98	−45.03

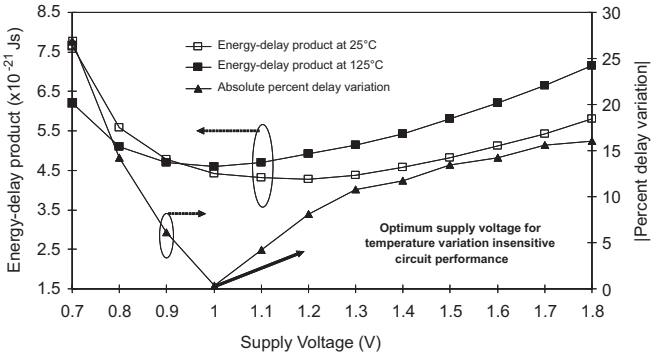

Fig. 10. The energy-delay product at two different temperatures and the percent delay variation as a function of the supply voltage. The temperature is increased from 25 to 125 °C for an 8-bit array multiplier in the TSMC 180 nm CMOS technology.

circuit speed are, therefore, enhanced when the temperature is increased at supply voltages below the optimum supply voltage.

Energy-delay product at two different temperatures and percent delay variation when the temperature is increased from 25 to 125 °C for an 8-bit array multiplier in a 180 nm CMOS technology are shown as a function of the supply voltage in Fig. 10. For the supply voltages above the optimum supply voltage, the delay variations are determined primarily by the mobility variations. As listed in Table 2, the percent variation in carrier mobility is similar for a specific temperature range at different supply voltages. Alternatively, the sensitivity of gate overdrive to temperature variations is enhanced with the scaling of the supply voltage. As the supply voltage is scaled below the optimum supply voltage, therefore, the rate of increase of delay variations (determined primarily by the variations of the gate overdrive for $V_{DD} < V_{Optimum}$) is enhanced as shown in Fig. 10.

Due to the higher rate of change of delay below the optimum supply voltage, reduction in the propagation delay dominates the increase in energy in the EDP term as the temperature is increased. The energy-delay product at 125 °C is, therefore, lower than the energy-delay product at 25 °C for the supply voltages below the optimum supply voltage, as illustrated in Fig. 10. Consequently, the worst case energy-delay product is exhibited at a lower temperature in ultra-low-voltage circuits operating at supply voltages below the optimum supply voltage.

In some applications lower energy consumption is the primary goal rather than higher speed. The energy consumed per cycle is

$$\text{Energy}_{\text{Total}} \approx \text{Energy}_{\text{Switching}} + \text{Energy}_{\text{Leakage}} \tag{12}$$

$$\text{Energy}_{\text{Switching}} \propto V_{DD}^2 \tag{13}$$

$$\text{Energy}_{\text{Leakage}} = I_{\text{Leakage}} V_{DD} T_c \tag{14}$$

where $\text{Energy}_{\text{Total}}$, $\text{Energy}_{\text{Switching}}$, $\text{Energy}_{\text{Leakage}}$, and I_{Leakage} are the total energy consumed per cycle, total dynamic switching energy per cycle, total leakage energy per cycle, and total leakage current, respectively.

The normalized energy profile of a 16-bit Brent–Kung adder in a 180 nm CMOS technology is shown as a function of the supply voltage at 25 and 125 °C in Figs. 11 and 12, respectively. Similarly, the energy profile of the adder in a 65 nm CMOS technology at 25 and 125 °C is shown in Figs. 13 and 14, respectively. Scaling the supply voltage reduces the dynamic switching energy, as given by (13). Scaling the supply voltage, however, also increases the total leakage energy per cycle as given by (14), due to the increase in the clock period [16]. The total energy consumption, therefore, has a minimum as shown in Figs. 11–14.

The supply voltage that provides minimum energy is determined by the relative significance of dynamic switching and leakage energy components [16]. In a 180 nm CMOS technology, the minimum energy consumption at 25 °C is observed in the subthreshold region

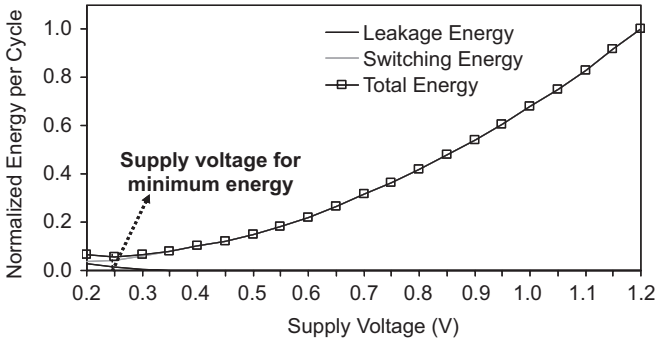

Fig. 11. Normalized switching, leakage, and total energy as a function of the supply voltage at 25 °C for a 16-bit Brent–Kung adder in the TSMC 180 nm CMOS technology.

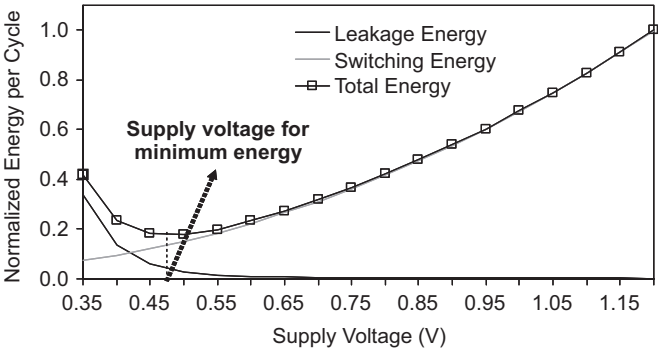

Fig. 12. Normalized switching, leakage, and total energy as a function of the supply voltage at 125 °C for a 16-bit Brent–Kung adder in the TSMC 180 nm CMOS technology.

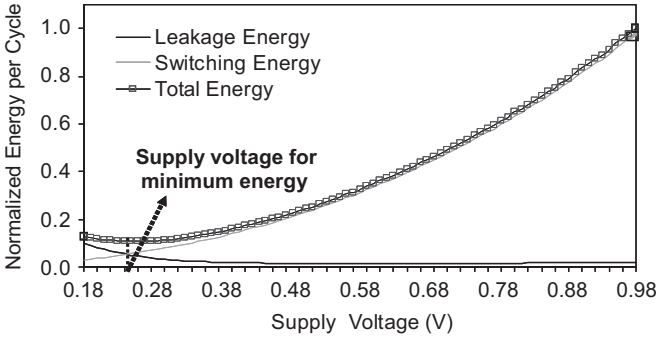

Fig. 13. Normalized switching, leakage, and total energy as a function of the supply voltage at 25 °C for a 16-bit Brent–Kung adder in the predictive 65 nm CMOS technology.

($V_{DD} < |V_{t0}| = 0.46$ V), as shown in Fig. 11. Leakage current increases at higher temperatures due to the reduction in device threshold voltages and the enhancement of the thermal voltage [18]. The supply voltage that minimizes the energy consumption is higher for circuits with relatively higher leakage currents [16]. The energy consumption at 125 °C is minimized when the circuits in a 180 nm CMOS technology are operated in the strong inversion region ($V_{DD} > |V_{t0}| = 0.46$ V), as shown in Fig. 12.

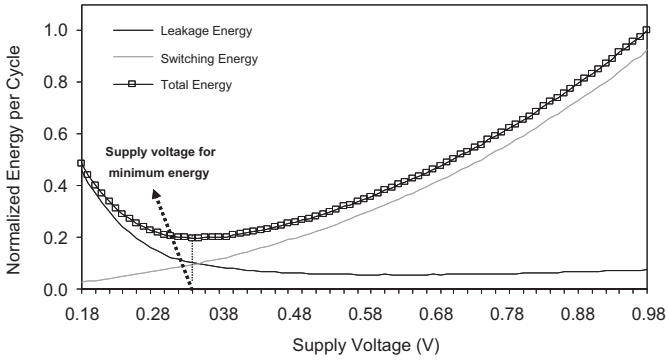

Fig. 14. Normalized switching, leakage, and total energy as a function of the supply voltage at 125 °C for a 16-bit Brent–Kung adder in the predictive 65 nm CMOS technology.

Supply voltage, threshold voltage, and gate-oxide thickness of MOSFETs are scaled with each new technology generation [18]. Supply voltage scaling reduces the dynamic energy component. Alternatively, the scaling of threshold voltage and gate-oxide thickness increases the leakage energy. The dynamic energy to leakage energy ratio is, therefore, reduced with each new technology generation. The increased leakage energy per switching cycle shifts the regime where the energy is minimized in a deeply scaled CMOS technology. For the circuits in this 65 nm CMOS technology with significant leakage current, the minimum energy consumption is observed in the strong inversion region ($V_{DD} > |V_{t0}| = 0.22$ V) as shown in Figs. 13 and 14.

The energy and propagation delay of circuits operating at the nominal supply voltage are listed in Table 3. The energy and propagation delay at the optimum supply voltages providing temperature variation insensitive propagation delay, minimum energy-delay product, and minimum energy for circuits in 180 and 65 nm CMOS technologies are listed in Tables 4 and 5, respectively. The energy and delay at the different supply voltages are normalized to the energy and propagation delay of the corresponding circuit at the room temperature (25 °C) and the nominal supply voltage in Tables 4 and 5.

As listed in Table 4, the propagation delay of circuits in a 180 nm CMOS technology varies up to 6.1% and 92.7% when the temperature is increased from 25 to 125 °C at the supply voltages providing minimum energy-delay product and minimum energy, respectively. Similarly, as listed in Table 5, the propagation delays of circuits in a 65 nm CMOS technology vary by up to 50% and 33% when the temperature is increased at the supply voltages that yield minimum energy-delay product and minimum energy, respectively. Therefore, similar to the high-speed integrated circuits operating at the nominal supply voltage, propagation delay of low-power integrated circuits with deeply scaled supply voltages are also very sensitive to temperature fluctuations. In circuits optimized for minimum energy and minimum energy-delay product, within

Table 3
Delay and energy at the nominal supply voltage in 180 and 65 nm CMOS technologies

CMOS node	Nominal supply voltage (V)		Temperature (°C)	16-Bit Brent–Kung adder	8-Bit array multiplier	16-Bit ripple carry adder
180 nm	1.8	Delay (ps)	25	1264.4	2126.2	2891.8
			125	1423.2	2465.0	3238.3
		Energy (fJ)	25	1934.2	2732.7	1692.1
			125	1966.6	2897.4	1722.3
65 nm	1.0	Delay (ps)	25	633.3	1015.9	1470.7
			125	978.6	1563.8	2257.0
		Energy (fJ)	25	467.7	676.5	363.2
			125	506.8	852.5	415.8

die temperature variations due to unbalanced switching activity would typically be small. The primary source of temperature fluctuations in an ultra low-power circuit with a scaled supply voltage would be the variation in the ambient temperature. A change in the ambient temperature can significantly alter the performance of an ultra-low-voltage circuit by affecting all the devices on a die equally.

6. Energy efficient temperature variation resilient CMOS circuits

The tradeoffs of attaining temperature variation resilience by operating a circuit at an optimum supply voltage are discussed in this section. The energy and propagation delay characteristics at the supply voltages that yield temperature variation insensitive circuit performance, minimum energy-delay product, and minimum energy are compared.

As listed in Table 4, the supply voltages that suppress the delay variations when the temperature fluctuates are similar to the supply voltages providing minimum energy-delay product in a 180 nm CMOS technology. Alternatively, the supply voltages that yield minimum energy are lower than the optimum supply voltages. The propagation delay, as compared to the delay at the nominal supply voltage, is up to 2.7× and 2.9× longer when circuits in a 180 nm CMOS technology are operated at the supply voltages for minimum energy-delay product (V_{DD} optimized for minimum EDP at 125 °C) and temperature variation insensitive circuit performance, respectively. At the supply voltages for minimum energy-delay product, the energy per cycle is 63.4–78.4% lower than the energy per cycle at the nominal supply voltage. Similarly, the energy per cycle at the optimum supply voltages that yield temperature variation insensitive circuit performance is 72.9–75.2% lower than the energy at the nominal supply voltage.

The minimum energy-delay product is 23–40% lower than the energy-delay product at the nominal supply voltage. Similarly, the energy-delay product at the optimum supply voltages that yield temperature variation insensitive circuit performance is 22–40% lower than the energy-delay product at the nominal supply voltage. The difference of the minimum achievable energy-delay product and the energy-delay product at the supply voltages for temperature variation insensitive circuit performance is less than 3%.

For circuits in a 65 nm CMOS technology, the supply voltages that yield temperature variation insensitive circuit performance and minimum energy are lower than the supply voltages providing minimum energy-delay product, as listed in Table 5. When the circuits are operated at the supply voltages for minimum energy, the circuit speed is degraded by up to 45.4× as compared to the speed at the nominal supply voltage. Similarly, the propagation delay at the temperature variation insensitive optimum supply voltages is up to 17.6× longer than the delay at the nominal supply voltage ($V_{DD} = 1.0$ V). The minimum achievable energy is 65–89% lower than the energy per switching cycle at the nominal supply voltage. Similarly, the energy at the temperature variation insensitive optimum supply voltages is 55–88% lower than the energy at the nominal supply voltage.

As illustrated with the data in Tables 4 and 5, low-power integrated circuits optimized for minimum energy or minimum energy-delay product are highly sensitive to temperature fluctuations. Alternatively, integrated circuits with supply voltages optimized for temperature fluctuation insensitive speed characteristics also display significantly reduced energy consumption or energy-delay product as compared to the circuits operating with the nominal supply voltage. Energy efficiency and temperature fluctuation tolerance are therefore simultaneously achieved with the proposed supply voltage optimization technique as compared to the traditional margin-based designs optimized for functionality at the worst case die temperature.

7. Threshold voltage optimization for temperature variation insensitive delay

The results presented in Sections 4–6 indicate that energy efficiency and temperature variation resilience in CMOS integrated circuits can be simultaneously achieved by employing the supply voltage optimization technique. A new design methodology based on optimizing the threshold voltages to suppress the propagation delay variations when

Table 4
Normalized delay and energy at the optimum supply voltage and the supply voltages providing minimum energy-delay product and minimum energy in a 180 nm CMOS technology

180 nm CMOS technology	Temperature (°C)	Supply voltage optimized for temperature variation insensitive delay			Supply voltage optimized for minimum energy-delay product at 25 °C			Supply voltage optimized for minimum energy-delay product at 125 °C			Supply voltage optimized for minimum energy at 25 °C			Supply voltage optimized for minimum energy at 125 °C		
		V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*
16-Bit Brent–Kung adder	25	0.96	2.76	0.27	1.07	2.16	0.34	0.92	3.08	0.25	0.25	10167.67	0.02	0.48	84.92	0.06
	125		2.76	0.27		2.25	0.34		3.02	0.25		742.07	1.06		30.16	0.07
8-Bit array multiplier	25	1.01	2.90	0.27	1.16	2.09	0.37	1.01	2.90	0.27	0.36	1826.80	0.04	0.58	34.30	0.08
	125		2.90	0.28		2.22	0.38		2.90	0.28		220.10	1.13		17.09	0.11
16-Bit ripple carry adder	25	0.96	2.73	0.25	1.08	2.08	0.32	0.90	3.22	0.22	0.27	5389.38	0.03	0.50	57.52	0.06
	125		2.73	0.25		2.18	0.33		3.12	0.22		510.96	0.97		23.39	0.08

E^*, normalized energy.

Table 5
Normalized delay and energy at the optimum supply voltage and the supply voltages providing minimum energy-delay product and minimum energy in a 65 nm CMOS technology

65 nm CMOS technology	Temperature (°C)	Supply voltage optimized for temperature variation insensitive delay			Supply voltage optimized for minimum energy-delay product at 25 °C			Supply voltage optimized for minimum energy-delay product at 125 °C			Supply voltage optimized for minimum energy at 25 °C			Supply voltage optimized for minimum energy at 125 °C		
		V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*
16-Bit Brent–Kung adder	25	0.32	17.6	0.12	0.59	2.1	0.32	0.60	2.0	0.34	0.25	45.4	0.11	0.34	12.7	0.13
	125		17.6	0.22		3.1	0.38		3.0	0.39		35.8	0.29		13.8	0.21
8-Bit array multiplier	25	0.33	16.8	0.19	0.68	1.7	0.42	0.71	1.6	0.46	0.34	14.8	0.19	0.47	4.3	0.23
	125		16.9	0.57		2.5	0.61		2.4	0.65		15.3	0.55		5.8	0.44
16-Bit ripple carry adder	25	0.32	17.6	0.14	0.63	1.8	0.35	0.63	1.8	0.35	0.31	18.9	0.14	0.41	6.0	0.17
	125		17.6	0.34		2.7	0.46		2.7	0.46		18.5	0.35		7.6	0.30

E^*, normalized energy.

the temperature fluctuates is evaluated in this section. The speed and energy tradeoffs with the supply and threshold voltage optimization techniques are compared.

For circuits operating at the nominal supply voltage, the gate overdrive sensitivity to temperature fluctuations can be enhanced by increasing the device threshold voltage. The threshold voltages of MOSFETs can be altered during fabrication by varying the substrate doping density [19,20] and/or varying the gate-oxide thickness [21]. The variation of the drain current (I_{DS}) with the device threshold voltage (V_{t0}) for devices in 180 and 65 nm CMOS technologies is shown in Figs. 15 and 16, respectively. At the optimum threshold voltage, temperature fluctuation induced gate overdrive variation counterbalances the carrier mobility variation. Similar to the optimum supply voltage operation, MOSFETs operating at the optimum threshold voltages produce temperature variation insensitive constant drain current, as shown in Figs. 15 and 16.

The optimum threshold voltages ($V_{t0\text{-opt}}$) that provide temperature variation insensitive speed are shown in Figs. 17 and 18. The NMOS and PMOS transistor threshold voltages are assumed to be equal ($V_{t0\text{-NMOS}} = |V_{t0\text{-PMOS}}|$) and scaled together in this paper. As shown in Fig. 17, circuits operating at the nominal supply voltage in a 180 nm CMOS technology are insensitive to temperature

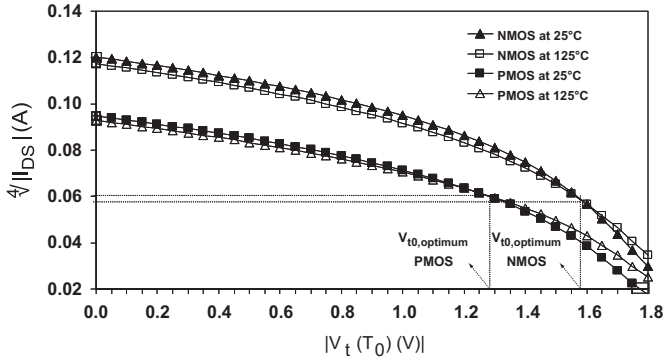

Fig. 15. Variation of MOSFET drain current with threshold voltage and temperature in the TSMC 180 nm CMOS technology. $|V_{DS}| = |V_{GS}| = V_{DD} = 1.8$ V.

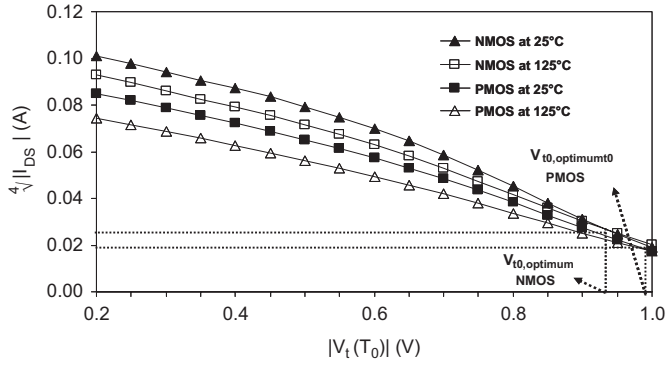

Fig. 16. Variation of MOSFET drain current with threshold voltage and temperature in the predictive 65 nm CMOS technology. $|V_{DS}| = |V_{GS}| = V_{DD} = 1.0$ V.

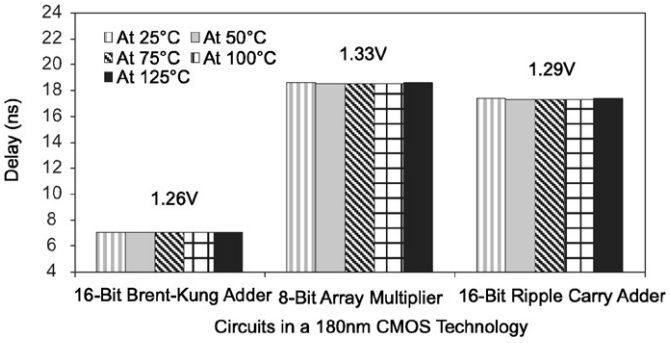

Fig. 17. Optimum threshold voltages that achieve temperature variation insensitive speed characteristics in the TSMC 180 nm CMOS technology.

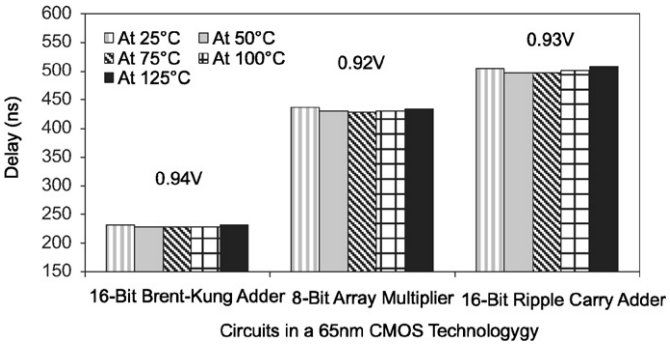

Fig. 18. Optimum threshold voltages that achieve temperature variation insensitive speed characteristics in the predictive 65 nm CMOS technology.

variations when the threshold voltage is 2.7× to 2.9× higher than the nominal device threshold voltage ($|V_{t0\text{-nominal}}| = 0.46$ V). Similarly, the delay variations of circuits operating at the nominal supply voltage in a 65 nm CMOS technology are suppressed when the device threshold voltage is 4.2× to 4.3× higher than the nominal device threshold voltage ($|V_{t0\text{-nominal}}| = 0.22$ V), as shown in Fig. 18.

The temperature variation insensitive drain current produced by a MOSFET with an optimum threshold voltage is smaller as compared to the drain current at the optimum supply voltage, as shown in Figs. 3, 4, 15, and 16. The speed penalty with the threshold voltage optimization technique is, therefore, higher as compared to the supply voltage optimization technique. As shown in Figs. 7 and 17, the speed at the optimum supply voltage is up to 3× higher, as compared to the speed at the optimum threshold voltages in a 180 nm CMOS technology. Similarly, as shown in Figs. 8 and 18, the propagation delay is up to 25.6× higher when circuits in a 65 nm CMOS technology are operated at the optimum threshold voltages as compared to the circuits operating at the optimum supply voltage.

The energy consumptions at the optimum threshold voltages that achieve temperature variation insensitive circuit performance are listed in Table 6. The energy per switching cycle at different threshold voltages are

Table 6
Normalized energy at the optimum threshold voltages in 180 and 65 nm CMOS technologies

CMOS technology	Temperature (°C)	16-Bit Brent–Kung adder	8-Bit array multiplier	16-Bit ripple carry adder
180 nm	$\lvert V_{t0}(T_0)\rvert$	1.26	1.33	1.29
	25	0.84	0.77	0.83
	125	0.84	0.78	0.83
65 nm	$\lvert V_{t0}(T_0)\rvert$	0.94	0.92	0.93
	25	0.90	0.79	0.85
	125	0.91	0.83	0.86

normalized to the energy of the corresponding circuit at the nominal voltages (nominal V_{DD} and V_t) and room temperature (25 °C). Supply voltage scaling lowers both leakage and dynamic switching energy [18]. Alternatively, increasing the device threshold voltage at the nominal supply voltage lowers only the leakage energy while maintaining the switching energy. The energy savings are, therefore, lower at the optimum threshold voltages as compared to the optimum supply voltage that provides temperature variation insensitive speed. At the optimum supply and threshold voltages, the energy per switching cycle is reduced by up to 4× and 1.3×, respectively, as compared to the energy at the nominal supply voltage in a 180 nm CMOS technology. Similarly, the energy at the optimum supply and threshold voltages is lower by up to 8.6× and 1.3×, respectively, as compared to the energy at the nominal supply voltage for circuits in a 65 nm CMOS technology. The energy consumed at the optimum threshold voltage is higher than the energy per cycle at the optimum supply voltage by up to 3.3× and 7.7× for circuits in 180 and 65 nm CMOS technologies, respectively.

Higher supply voltages are preferable in speed critical applications. The performance degradation with the threshold voltage optimization technique diminishes the potential speed gains by employing a higher nominal supply voltage. Furthermore, energy savings achieved by the threshold voltage optimization technique is lower as compared to the supply voltage optimization technique. The supply voltage optimization technique is therefore more effective in simultaneously achieving energy efficiency and temperature variation tolerance with a smaller speed penalty as compared to the threshold voltage optimization technique in CMOS integrated circuits.

8. Conclusions

A design methodology based on optimizing the supply voltage for simultaneously achieving energy efficiency and temperature variation insensitive circuit performance is presented in this paper. Temperature dependent device parameters that cause variations in MOSFET drain current are identified. When operating at the nominal supply voltage, the speed of circuits degrades by up to 15.9% and 54.5% as the temperature is increased from 25 to 125 °C in the 180 and 65 nm CMOS technologies, respectively.

Operating an integrated circuit at the prescribed nominal supply voltage is not preferable for reliable circuit operation under temperature fluctuations. Circuits display a temperature variation insensitive propagation delay when operated at a supply voltage 44–47% lower than the nominal supply voltage in a 180 nm CMOS technology. Similarly, the optimum supply voltages are 67–68% lower than the nominal supply voltage for circuits in a 65 nm CMOS technology.

Circuits optimized for minimum energy or minimum energy-delay product exhibit high sensitivity to temperature fluctuations. Alternatively, integrated circuits with supply voltages optimized for temperature fluctuation insensitive speed characteristics also display significantly reduced energy-delay product and energy consumption. Low-power operation and delay insensitivity to temperature fluctuations can therefore be simultaneously achieved with the proposed supply voltage optimization technique.

A new design methodology based on threshold voltage optimization to suppress the propagation delay variations when the temperature fluctuates is also proposed in this paper. Circuits operating at the nominal supply voltage in a 180 nm CMOS technology are insensitive to temperature variations when the threshold voltage is 2.7× to 2.9× higher than the nominal device threshold voltage. Similarly, the delay variations of circuits in a 65 nm CMOS technology operating at the nominal supply voltage are suppressed when the device threshold voltage is 4.2× to 4.3× higher than the nominal device threshold voltage. The speed and energy tradeoffs with the two different optimization techniques are compared. The supply voltage optimization technique is shown to be more effective in providing temperature variation tolerance with a smaller speed penalty and lower energy consumption as compared to the threshold voltage optimization scheme.

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