Dual Signal Frequencies and Voltage Levels for Low Power and Temperature-Gradient Tolerant Clock Distribution

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ABSTRACT

A methodology based on supply voltage and frequency scaling for lowering the power consumption and temperature fluctuations induced skew of clock distribution networks is proposed in this paper. The clock signal is distributed globally at a scaled supply voltage and frequency. The optimum supply voltage that minimizes clock skew is 44% less than the nominal supply voltage in a 0.18μm CMOS technology. Combined frequency multiplier and level converter circuits are utilized at the leaves of the clock tree for restoring the standard full voltage swing clock signal with the higher target clock frequency in order to maintain the performance of the system. A novel dual-threshold-voltage frequency doubler with voltage level conversion capability, suppressed temperature fluctuations sensitivity, and low power consumption characteristics is presented. The temperature fluctuations induced skew and power consumption of the proposed dual-V_{DD}/dual-frequency clock distribution network are reduced by up to 80% and 76%, respectively, as compared to a standard distribution network operating at the nominal supply voltage with the target system clock frequency.

Categories and Subject Descriptors

B.7.m [Integrated Circuits]: Miscellaneous

General Terms

Design

Keywords

Temperature Variations, Supply Voltage Scaling, Frequency Scaling, Clock Skew, Dual-V_{DD}, Dual-V_{th}.

1. INTRODUCTION

Clock distribution network (CDN) consumes a significant portion of the power, area, and metal resources of an integrated circuit (IC). Technology scaling coupled with the increase in die size and clock frequency causes the process and environment parameter variations to be more pronounced [1]. Coping with parameter variations is particularly challenging in the design of the clock distribution networks since the clock signal needs to be distributed to the entire IC with controlled skew. Clock skew degrades the performance of an IC by reducing the time available for computation in each clock cycle.

Due to the imbalanced utilization and diversity of circuitry, time-varying temperature gradients occur across an IC. The effect of on-chip temperature gradients on clock skew is characterized in this paper. Supply voltage optimization is demonstrated to be an effective method for minimizing the clock skew induced by temperature fluctuations in a clock distribution network. The clock signal is distributed at a scaled optimum supply voltage with the proposed scheme. At the low optimum supply voltage the signal transition times at the outputs of the clock buffers are increased. To maintain the target clock frequency while satisfying the transition time constraint (transition time << clock period) the size of the buffers are increased. With this technique, the performance of the system is maintained by restoring the clock signal voltage amplitude to the standard higher voltage level by employing level converters at the leaves of the low voltage clock distribution network. An alternative technique with potentially lower power consumption is to scale the clock frequency together with the supply voltage. With this second approach the system performance is maintained by employing frequency multipliers and level converters at the leaves of the low-voltage/low-frequency clock distribution network. Both techniques are characterized for power consumption and temperature fluctuations induced clock skew in this paper. A novel hybrid dual-threshold-voltage frequency doubler and level converter circuit with suppressed delay sensitivity to temperature fluctuations and low power consumption characteristics is proposed.

The paper is organized as follows. Previous works on low skew and low power clock distribution networks are reviewed in Section 2. The proposed dual-V_{DD}/dual-frequency clocking methodology is presented in Section 3. Finally, conclusions are provided in Section 4.

2. PREVIOUS WORKS

The enhanced operating frequency and growing die size of ICs increase the power consumption of the clock distribution network while shrinking the timing budget for clock skew with each new technology generation. The two primary issues in the design of clock distribution networks are the higher power consumption and the increased clock skew due to the parameter variations in today's high performance integrated circuits.

Three primary approaches for reducing clock skew can be identified in the literature. With the first approach, the clock distribution network topology is designed for enhanced robustness against process parameter variations [2]. However, the clock skew due to environment variations, caused by the fluctuations of the temperature and the supply voltage, is ignored in [2]. With the second approach presented in [3], programmable delay elements are employed for reducing the skew induced by process parameter

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variations in a clock distribution network. The delay elements are programmed in order to shift the characteristics of a fabricated IC towards the target design specifications. This approach, however, lacks the dynamic tuning capability required to cope with the environment variations. With the third approach presented in [4] and [5], the delay elements are programmed dynamically using phase detectors in a clock distribution network. Using programmable delay elements with phase detectors is potentially effective in reducing the deviations in circuit characteristics induced by both process and environment parameter variations. This approach, however, suffers from higher design complexity, area, power consumption, and clock jitter.

Low-swing clocking is proposed in [6]–[8] to reduce the power consumption. Level converters regenerate the full swing clock signal at the clock utilization points in order to maintain the performance of the system. The additional power consumption and skew overhead caused by the level converters is not addressed in [7]. In [6], the effect of temperature fluctuations on clock skew is not considered. In [8], although the power consumption is reduced, the clock distribution network becomes more sensitive to supply voltage and temperature variations. The weaker driving capability of the low voltage buffers requires increasing either the number or the size of the buffers to maintain the clock signal slew rate. The increased number or size of the buffers causes additional power consumption. Neither this power overhead is evaluated nor a methodology for supply voltage optimization is presented in [6]–[8].

A dual-V_{DD} clock distribution network to suppress the clock skew induced by on-chip temperature gradients is proposed in [9]. The clock signal is globally distributed at a lower optimum supply voltage for minimizing the temperature fluctuations induced skew. Level converters restore the full swing clock signal at the leaves of the clock distribution network in order to maintain the system performance. 74% and 50.8% reduction in the temperature fluctuations induced clock skew and the power consumption, respectively, as compared to a standard single-V_{DD} clock distribution network is reported in [9]. With this single-frequency clocking technique, however, the target clock frequency and the associated tight slew rates are maintained by significantly increasing the size of the buffers in the low-voltage clock tree, thereby degrading the potential power savings that could be attained with voltage scaling.

In this paper, a new methodology based on dual-V_{DD} and dual-frequency clocking is proposed for simultaneously suppressing the power consumption and the temperature fluctuations induced skew in the clock distribution networks. Distributing the clock signal at a lower optimum supply voltage minimizes the source-to-sink propagation delay variations due to on-chip temperature gradients. To maintain the clock signal integrity (sharp signal transition times relative to the clock period) and to further reduce the power consumption, the clock signal is distributed globally at half the target frequency. The need for buffer resizing for high frequency operation at low-V_{DD} is eliminated by simultaneous supply voltage and frequency scaling. Frequency multipliers with level conversion capability are utilized at the leaves of the clock distribution network for restoring the full voltage swing clock signal with the target clock frequency in order to maintain the system performance. A novel dual-threshold-voltage hybrid frequency-doubler/level-converter circuit with suppressed delay sensitivity to temperature fluctuations and low power consumption characteristics is also proposed in this paper.

3. SUPPLY VOLTAGE OPTIMIZATION IN CLOCK DISTRIBUTION NETWORKS

The effect of on-chip temperature gradients on clock skew is characterized in this section. The dual-V_{DD}/single-frequency clocking methodology for lowering the temperature fluctuations induced clock skew is presented in Section 3.1. The new dual-V_{DD}/dual-frequency clocking methodology providing enhanced power savings while effectively suppressing the skew induced by temperature fluctuations is described in Section 3.2.

A two-level buffered H-tree clock distribution network spanning a 20mm × 20mm die in a 0.18μm CMOS technology is used for the evaluation of the methodologies presented in this paper, as shown in Fig. 1. The target clock frequency is 1 GHz. The thick and thin lines in Fig. 1 represent the first (routed in the topmost metal layer) and the second (routed in the second topmost metal layer) levels, respectively, of the clock distribution network. Each branch in the first (second) level is 5mm (2.5mm) long. Each wire segment between two buffers is modeled as a π2 RC network. The wire width is 1μm (0.5μm) in the first (second) topmost metal layer. The wire thickness is 1μm. The spacing between wires is 1μm. The sheet resistance is 0.02Ω/□. Buffer insertion and sizing are carried out using an iterative Spice-based algorithm assuming a uniform die temperature. The objective of the algorithm is to minimize the power consumption while constraining the transition times of the clock signal at the leaves of the clock tree to be less than 10% of the clock period. The standard clock distribution network, shown in Fig. 1, is designed at the nominal supply voltage ($V_{DD\text{-}nominal}$ = 1.8V) assuming a uniform worst-case die temperature of 125 °C.

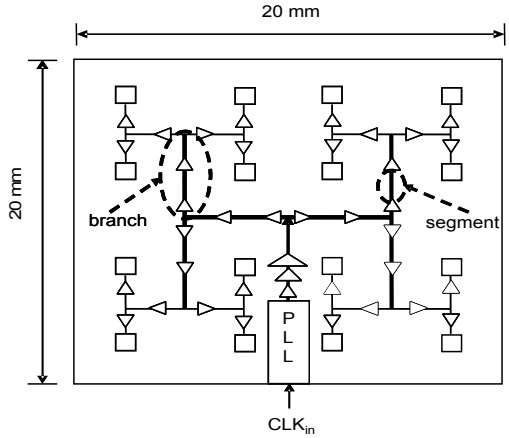

Fig. 1. Two level buffered H-tree clock distribution network.

Due to on-chip temperature gradients, paths emerging from the root of a clock distribution network pass through different temperature zones, thereby producing temperature fluctuations induced clock skew. The temperature profile of an IC varies over time. Four on-chip temperature profiles, as shown in Fig. 2, are considered for characterizing the temperature fluctuations induced clock skew. Both vertical and horizontal temperature gradients are considered with a relatively different location for the hottest spot in each temperature profile. The die temperature range is 25 °C (room temperature) to 125 °C. The temperature fluctuations induced clock skew and the power consumption of the standard clock distribution network are listed in Table 1 for each temperature profile. The highest clock skew is observed with the second and the fourth temperature profiles, as listed in Table 1.

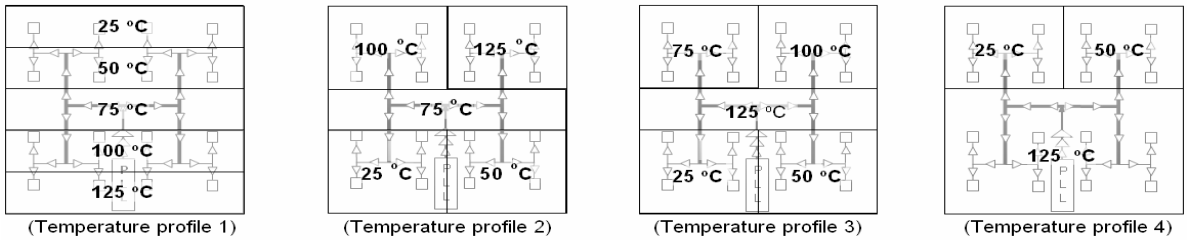

Fig. 2. Four different on-chip temperature profiles considered in this paper.

Table 1. Temperature fluctuations induced clock skew and power consumption of the standard single-V_{DD} / single-frequency CDN

Temperature Profile	Skew (ps)		Power Consumption (mW)
	Rising Edge	Falling Edge	
1	35.0	32.50	13.440
2	54.6	51.88	13.443
3	40.7	38.50	13.448
4	54.7	51.76	13.470

The effect of temperature fluctuations on wire and gate delays is explained next. An increase in the temperature degrades the absolute values of the threshold voltage and the carrier mobility of a MOSFET. The degradation of the threshold voltage tends to enhance the MOSFET drain current because of the increase in the gate overdrive $|V_{GS}-V_{th}|$. Alternatively, the degradation of the carrier mobility tends to lower the MOSFET drain current [10]. Variations of the gate overdrive are less significant as compared to the carrier mobility variations when the temperature fluctuates in circuits operating at the nominal supply voltage in a 0.18µm CMOS technology. Drain current is therefore reduced causing an increase in the gate delay at a higher temperature. Furthermore, the resistance of metal wires increases linearly with the temperature. The signal propagation delays along wires as well as the gate delays therefore increase at elevated die temperatures.

The variation of the gate overdrive with the temperature is enhanced at a lower supply voltage and/or a higher $|V_{th}|$ as described in [10]. At an optimum supply or threshold voltage, the gate overdrive variations counterbalance the mobility variations, thereby producing a temperature fluctuations insensitive constant transistor current and circuit delay. This counterbalancing of the mobility variations through voltage optimization is exploited in order to lower the temperature fluctuations induced clock skew with the methodologies presented in Sections 3.1 and 3.2.

3.1 Dual-V_{DD}/Single-Frequency Clocking Methodology

A methodology based on supply voltage optimization to minimize the temperature fluctuations induced clock skew while reducing the power consumption is presented in this section. Supply voltage optimization is performed by reducing the supply voltage with steps of 0.1V. The entire clock distribution network is redesigned at each scaled supply voltage to maintain the target clock frequency while satisfying the transition time constraints assuming a uniform worst-case die temperature. The clock distribution networks designed for different V_{DD} are then characterized for skew and power consumption. The maximum clock skew between the leaves of the clock distribution network and the average power consumed by the network are computed at each supply voltage for different temperature profiles.

The maximum clock skew between the leaves of the clock distribution network versus the supply voltage is plotted in Figs. 3 and 4 for the rising and the falling edges of the clock signal, respectively. There is a common optimum supply voltage ($V_{DD-optimum}$ = 1V) at which the temperature fluctuations induced clock skew is minimized for all four temperature profiles as shown in Figs. 3 and 4. The temperature fluctuations induced clock skew is reduced by up to 80% with the supply voltage optimization scheme as compared to the standard clock distribution network operating at $V_{DD-nominal}$.

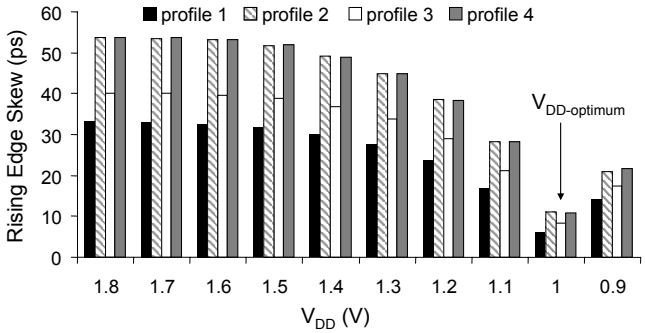

Fig. 3. Temperature fluctuations induced clock skew (for the rising edge) versus the supply voltage. $V_{DD-nominal}$ = 1.8V.

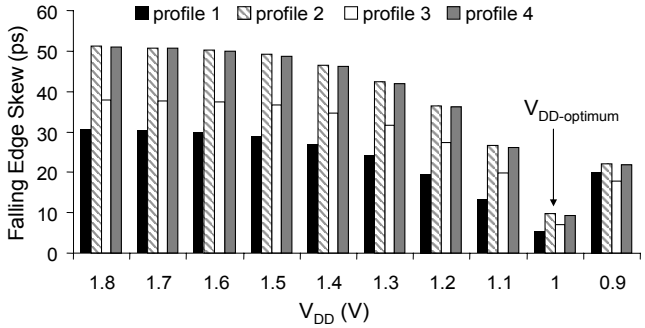

Fig. 4. Temperature fluctuations induced clock skew (for the falling edge) versus the supply voltage. $V_{DD-nominal}$ = 1.8V.

The variation of the normalized power consumption with the supply voltage is shown in Fig. 5. Buffer sizes are increased at the lower supply voltages to maintain the target clock frequency and the signal slew rates. Hence the reduction in average power consumption with the scaling of the supply voltage is less than quadratic. As the supply voltage is scaled, the power overhead of the larger buffers eventually exceeds the power savings obtained by reducing the supply voltage. There is therefore an optimum supply voltage that minimizes the power consumption. The optimum supply voltage ($V_{DD-optimum}$ = 1V) that minimizes the temperature fluctuations induced skew also minimizes the power consumption for this specific clock distribution network. A 53.8% reduction in the average power consumption is observed at the optimum supply voltage with the dual-V_{DD}/single-frequency clocking technique.

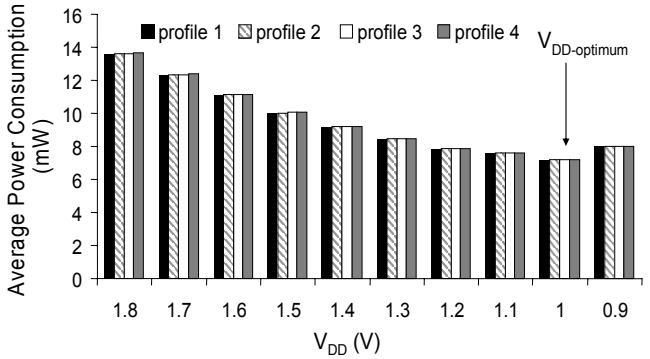

Fig. 5. Average power consumption of the clock distribution network versus the supply voltage for four different temperature profiles.

Level converters are utilized at the leaves of the clock tree for restoring the full voltage swing clock signal in order to maintain the system performance [9]. The temperature fluctuations induced clock skew and the power consumption of the dual-V_{DD}/single-frequency clock distribution network are listed in Table 2 with the overhead of the level converters included. The power consumption and temperature fluctuations induced clock skew of a CDN based on the dual-V_{DD}/single-frequency clocking methodology are reduced by up to 50.6% and 76%, respectively, as compared to the standard CDN, as listed in Tables 1 and 2.

Table 2. Temperature fluctuations induced clock skew and power consumption of the dual-V_{DD}/single-frequency CDN

Temperature Profile	Skew (ps)		Power Consumption (mW)
	Rising Edge	Falling Edge	
1	9	9	6.65
2	13	14	6.65
3	9	10	6.65
4	13	12	6.65

3.2 Dual-V_{DD}/Dual-Frequency Clocking Methodology

Maintaining the clock frequency of a low voltage clock distribution network requires increasing the sizes of the clock buffers, thereby degrading the potential power savings achievable with voltage scaling. A new voltage scaling methodology based on dual-V_{DD}/dual-frequency clocking is presented in this section for more effectively suppressing the temperature fluctuations induced clock skew while further reducing the power consumption.

The clock signal is distributed globally at a scaled optimum supply voltage for temperature fluctuations insensitivity. The clock frequency is scaled together with the supply voltage for enhanced power savings with the new technique. By halving the clock frequency in the global part of the clock tree, buffer resizing is avoided when the supply voltage is scaled, thereby further reducing the power consumption as compared to the dual-V_{DD}/single-frequency clocking methodology. New hybrid frequency doublers with built-in level conversion capability are employed at the leaves of the clock tree in order to restore the clock signal voltage amplitude to the standard full voltage swing with the higher target clock frequency required to maintain the system performance. Threshold voltage optimization is effectively applied to further suppress the temperature fluctuations induced skew at the leaves of the clock tree. The proposed methodology based on simultaneous voltage and frequency scaling is illustrated in Fig. 6.

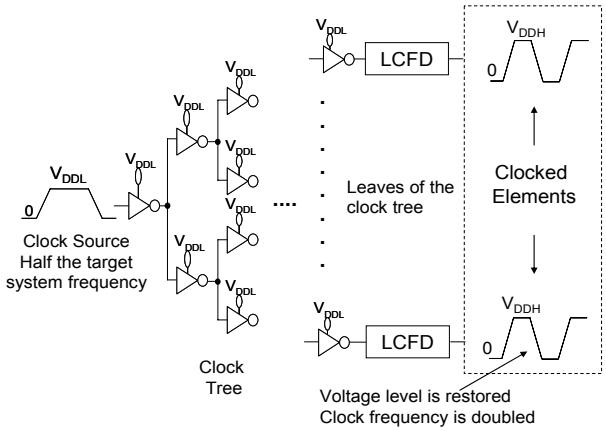

Fig. 6. The proposed dual-V_{DD}/dual-frequency clock distribution technique. LCFD: hybrid level-converter/frequency-doubler. V_{DDL}: low optimum supply voltage that minimizes the clock skew. V_{DDH}: nominal higher supply voltage required by the clocked elements for high speed.

A new frequency doubler with built-in level conversion capability based on a dual-threshold-voltage CMOS technology is proposed in this paper. The circuit consumes lower power while providing enhanced tolerance to temperature fluctuations as compared to the previously published circuits. The proposed circuit is shown in Fig. 7. V_{DDL} is the lower optimum supply voltage that minimizes skew (V_{DDL} = 1V in a 0.18μm CMOS technology) while V_{DDH} is the nominal supply voltage required by the clocked elements for high-speed operation (V_{DDH} = 1.8V in a 0.18μm CMOS technology).

The waveforms of the frequency doubler produced by HSPICE simulations are depicted in Fig. 8. The frequency doubler has two branches aimed at producing two consecutive negative pulses at the inputs of N_3 within each clock period of the input signal (V_{in}). The upper branch is composed of a delay element and N_1. This branch produces a negative pulse at $Node_4$ with the rising and falling edges of the signals at $Node_3$ and $Node_1$, respectively, as illustrated in Fig. 8. The lower branch is composed of the inverters I_2 and I_3 and the NAND gate N_2. This branch produces a negative pulse at $Node_6$ with the rising and falling edges of the signals at $Node_5$ and $Node_2$, respectively. The output of the frequency doubler is obtained by propagating the signals on the upper and the lower branches ($Node_4$ and $Node_6$) through N_3. The width of the pulses of the signals at $Node_4$ and $Node_6$ should be one quarter of the input period in order to produce an output signal with a 50% duty cycle. This requirement is achieved by the delay element shown in Fig. 9 designed to have a propagation delay of one quarter of the input period. The delay element is tuned by adjusting the number of stages and the values of the capacitors. The capacitors are implemented by transistors. The lower branch of the frequency doubler has an extra inverter delay as compared to the upper branch. The delays of the upper and lower branches are balanced by transistor sizing and by adding a capacitor to $Node_4$. N_2 is sized larger than N_1. Furthermore, the transistors in N_3 that are driven by $Node_6$ are sized larger than the transistors that are driven by $Node_4$ for balancing the delays of the upper and the lower branches.

Level conversion is achieved without feedback using high-$|V_{th}|$ PMOS transistors [12]. The low nominal zero-body-bias long-channel threshold voltages of the NMOS and PMOS transistors are 0.47V and -0.46V, respectively, in this 0.18μm CMOS technology.

Three different locations are considered for level conversion with the proposed frequency doubler as illustrated in Fig. 7. With the first proposed circuit (LCFD1), the level conversion is performed by I_1 (high-V_{th} = -1.26V). All the gates in LCFD1 operate with the higher supply voltage (V_{DDH}), thereby causing high power consumption. Furthermore, V_{DDH} is significantly higher than the optimum voltage required for temperature variations insensitive delay characteristics in this technology. LCFD1 therefore also suffers from significant delay variations.

Level conversion is performed by N_3 with the second proposed circuit (LCFD2). All the gates except N_3 operate with the lower optimum supply voltage V_{DDL}, thereby suppressing the power consumption as well as the skew up to the last circuit stage. Although N_3 is connected to the higher supply voltage, the threshold voltages of the PMOS devices in N_3 are optimized for suppressing the temperature fluctuations induced delay variations ($V_{thp\text{-}optimum}$ = -1.26V). The low current driving capability of N_3, however, requires the addition of an extra inverter at the output in order to satisfy the slew rate constraint of the clock signal. This extra gate causes additional power consumption and skew in LCFD2.

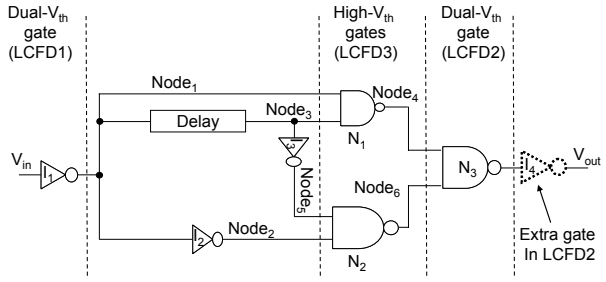

Fig. 7. Proposed hybrid level-converter/frequency-doubler. The dual-V_{th} gate(s) and all the downstream gates after the dual-V_{th} gate(s) operate with V_{DDH}.

Level conversion is performed by N_1 and N_2 with the third proposed circuit (LCFD3), as shown in Fig. 10. LCFD3 consumes lower power as well as exhibiting weaker sensitivity to temperature fluctuations. I_1, I_2, I_3, and the delay element are driven by the optimum supply voltage (V_{DDL}) that provides temperature fluctuations insensitive delay characteristics. The pull-down networks of N_1 and N_2 are driven by low-swing signals with the optimum voltage amplitude. The threshold voltages of the pull-down transistors in N_1 and N_2 are further optimized ($V_{thn\text{-}optimum}$ = 0.72V) in order to compensate for the delay variations of N_3 (for minimizing the accumulated delay variations of the multi-stage frequency doubler rather than only one circuit stage). Although the pull-up transistors in N_1 and N_2 are connected to the nominal supply voltage V_{DDH}, these transistors have high-$|V_{th}|$ optimized for temperature fluctuations insensitivity ($V_{thp\text{-}optimum}$ = -1.26V).

An alternative approach to the proposed hybrid level converter/frequency-doubler is to use separate circuits for level conversion and frequency multiplication. A standard single-V_{th} cascaded two-stage level-converter/frequency-doubler circuit (LCFD4) is shown in Fig. 11.

The following circuits are designed for a 1GHz output clock signal in a 0.18µm CMOS technology: LCFD1, LCFD2, LCFD3, and LCFD4. The delay variations of the circuits (for T: 25 °C → 125 °C) are characterized for odd and even pulses since the odd and even pulses of the output signal propagate through different paths in the frequency doublers. As listed in Table 3, LCFD3 displays the weakest delay sensitivity to temperature fluctuations and consumes the lowest power among the four level-converter/frequency-doubler circuits. The power consumption and the temperature fluctuation induced delay variation are reduced by up to 77% and 93%, respectively, with the proposed circuit LCFD3 as compared to the standard cascaded circuit LCFD4.

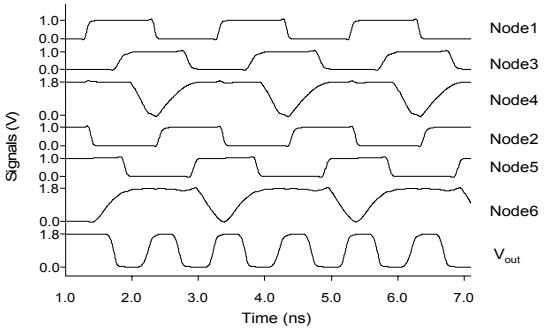

Fig. 8. Voltage waveforms of the frequency doubler (T = 25°C).

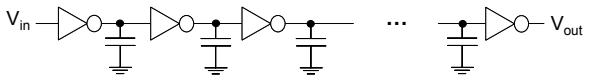

Fig. 9. The delay element.

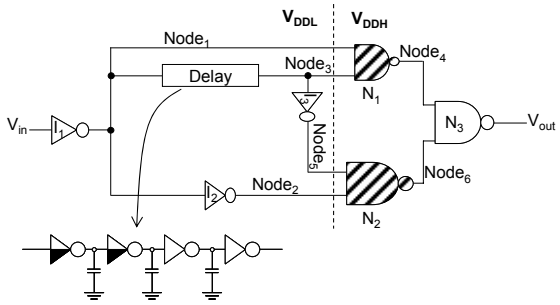

Fig. 10. LCFD3. The shaded NAND gates have high-V_{th} transistors. The shaded inverters have high-V_{th} NMOS transistors.

Table 3. Temperature fluctuations induced delay variation and power consumption of the level-converter/frequency-doubler circuits

Circuit	Delay Variation (ps)				Power Consumption (µW)
	Rising Edge		Falling Edge		
	Odd	Even	Odd	Even	
LCFD1	73	71	11	15	149
LCFD2	14	3	28	16	58.8
LCFD3	-6.6	-2.8	-2.9	1.7	53.5
LCFD4	99	83	29	45	237

* Negative sign indicates that the propagation delay is reduced at high temperature. Power measured at 125 °C.

The entire clock distribution network based on the proposed dual-V_{DD}/dual-frequency clocking methodology (with the LCFD3 circuits at the leaves) is characterized for temperature fluctuations induced skew and power consumption. The simulation results are listed in Table 4. The power consumption and temperature fluctuations induced skew of a CDN based on the proposed dual-V_{DD}/dual-frequency clocking methodology are reduced by up to 76% and 80%, respectively, as compared to the standard CDN.

As listed in Tables 2 and 4, the dual-V_{DD}/dual-frequency clocking methodology is more effective in reducing the overall power consumption and the temperature fluctuations induced clock skew as compared to the dual-V_{DD}/single-frequency clocking technique. With the new dual-V_{DD}/dual-frequency clocking

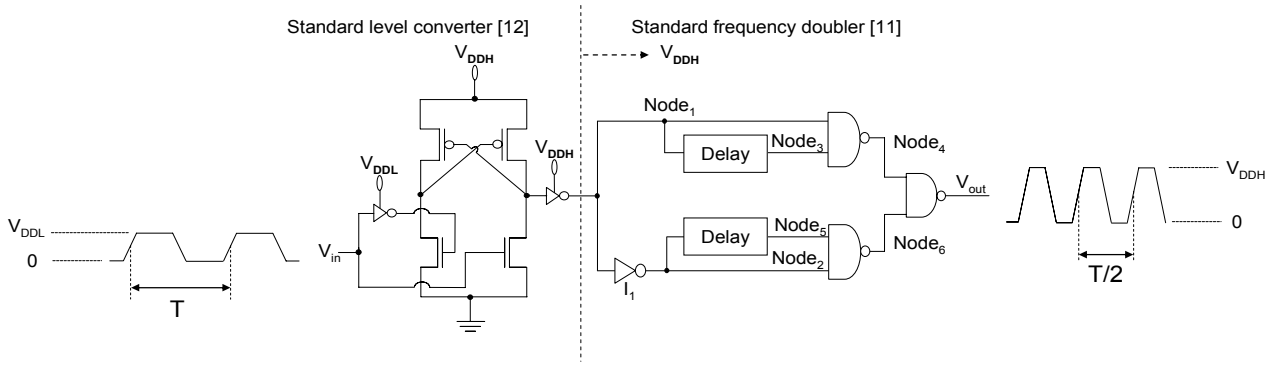

Fig. 11. A standard single-V_{th} cascaded two-stage level-converter/frequency-doubler circuit.

methodology, the power consumption and the clock skew are reduced by an additional amount of up to 52% and 22%, respectively, as compared to the dual-V_{DD}/single-frequency clocking methodology proposed in [9].

Table 4. Temperature fluctuations induced clock skew and power consumption of the proposed dual-V_{DD} /dual- frequency CDN

Temperature Profile	Skew (ps)				Power Consumption (mW)
	Rising Edge		Falling Edge		
	Odd	Even	Odd	Even	
1	6	6	7	7	3.207
2	5	13	13	13	3.207
3	3	8	8	10	3.207
4	4	12	12	13	3.208

4. CONCLUSIONS

A design methodology based on supply voltage and frequency scaling is proposed in this paper for simultaneously reducing the power consumption and the temperature fluctuations induced skew of clock distribution networks. The clock signal is distributed globally at a lower optimum supply voltage with half the target clock frequency. The optimum supply voltage that minimizes clock skew is 44% lower than the nominal supply voltage in a 0.18µm CMOS technology. Frequency multipliers and level converters are utilized at the leaves of the clock distribution network for restoring the standard full voltage swing clock signal with the target clock frequency in order to maintain the system performance. A new low-power dual-threshold-voltage frequency doubler with built-in voltage level conversion capability is presented. The proposed circuit displays robust delay characteristics under significant temperature fluctuations. Compared to an alternative two-stage single-V_{th} circuit composed of a standard level converter cascaded with a standard frequency doubler, the proposed hybrid circuit consumes 77% less power while producing 93% lower delay variation under temperature fluctuations. With the proposed dual-V_{DD}/dual-frequency clock distribution network, the temperature fluctuations induced clock skew and the power consumption are reduced by up to 80% and 76%, respectively, as compared to a standard clock distribution network operating at the nominal supply voltage and the target system clock frequency. The effectiveness of the proposed methodology for reducing skew and power consumption is verified with four different die temperature profiles.

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