Temperature Variation Insensitive Energy Efficient CMOS Circuits in a 65nm CMOS Technology

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Abstract – A design methodology based on optimizing the supply voltage for simultaneously achieving energy efficiency and temperature variation insensitive circuit performance is presented in this paper. Circuits exhibit temperature variation insensitive delay characteristics when operated at a supply voltage 67% to 68% lower than the nominal supply voltage. At scaled supply voltages, integrated circuits consume low power at the cost of reduced speed. The proposed design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance is, therefore, particularly attractive for low power applications with relaxed speed requirements. The supply voltages that yield minimum energy and minimum energy-delay product are identified at two different temperatures for circuits in a 65nm CMOS technology. The energy and speed at the supply voltages providing temperature variation insensitive propagation delay, minimum energy, and minimum energy-delay product are compared. Results indicate that energy efficient integrated circuits with deeply scaled supply voltages can also be made insensitive to temperature fluctuations by considering the temperature dependence of speed in the supply voltage optimization process.

1. INTRODUCTION

Process and environment parameter variations in scaled CMOS technologies are posing greater challenges in the design of reliable integrated circuits. Because of the imbalanced utilization and diversity of circuitry at different sections of an integrated circuit, temperature can vary significantly from one die area to another [1]. Furthermore, environmental temperature fluctuations can cause significant variations in die temperature. For example, electronic systems mounted on automobile engines operate at a temperature range from -40°C to 150°C [12]. Temperature variations affect the device characteristics of MOSFETs thereby varying the performance of integrated circuits.

The supply and threshold voltages are scaled with each new technology generation. The supply voltage is scaled primarily based on the device reliability and target clock frequency requirements in a new technology generation. Scaling the device dimensions strengthens the electric fields between device terminals while lowering the parasitic capacitances, thereby increasing the speed of CMOS integrated circuits. The speed of a circuit can be further enhanced by scaling the threshold voltages. Due to the subthreshold leakage power constraints, however, the threshold voltages are scaled at a much slower rate as compared to the supply voltage. The supply voltage to threshold voltage ratio is reduced with each new technology generation. The temperature fluctuation induced threshold voltage variation is therefore expected to have an increasingly important role in determining the MOSFET drain current variations when the temperature fluctuates. A complete reversal of temperature dependent speed characteristics of CMOS circuits is also likely to occur in the near future [2].

Temperature fluctuations alter threshold voltage, carrier mobility, and saturation velocity of a MOSFET [3]. Temperature fluctuation induced variations in individual device parameters have unique effects on MOSFET drain current. Propagation delay of a circuit is a function of the drain current produced by active transistors. Performance of an integrated circuit under temperature fluctuations is determined by the device parameter that dominates the MOSFET drain current variations.

There exists a bias voltage for which the device parameter variations counterbalance each other when the temperature fluctuates [2], [4], [9], [14]. The optimum supply voltages for temperature variation insensitive circuit performance are lower than the nominal supply voltage (V_{DD} = 1.0V) in a 65nm CMOS technology [14]. Integrated circuits operating at scaled supply voltages consume low power at the cost of reduced speed. The design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance is, therefore, particularly attractive in low power applications with relaxed speed requirements. In this paper, the supply voltages that achieve minimum energy and minimum energy-delay product are identified at two different temperatures for circuits in a 65nm CMOS technology. The energy and speed at the supply voltages providing temperature variation insensitive propagation delay, minimum energy, and minimum energy-delay product are compared. The speed and energy tradeoffs in the supply voltage optimization process are presented.

The paper is organized as follows. The influence of temperature dependent device parameters on the drain current of a MOSFET is analyzed in Section 2. Effect of temperature fluctuations on the device and circuit characteristics in a 65nm CMOS technology is examined in Section 3. The optimum supply voltages for temperature variation insensitive circuit performance are presented in Section 4. The supply voltages that yield minimum energy and minimum energy-delay product are identified in Section 5. The tradeoffs of supply voltage scaling are discussed in Section 6. Finally, some conclusions are given in Section 7.

2. MOSFET DRAIN CURRENT UNDER TEMPERATURE FLUCTUATIONS

Device parameters that are affected by temperature fluctuations, causing variations in drain current produced by a MOSFET, are identified in this section. BSIM4 device model

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is used for an accurate characterization of drain current in deeply scaled nanometer devices. The drain current of a MOSFET is [6]-[7]

$$I_{ds} \propto \frac{I_{ds\,0}}{1+\frac{R_{ds} I_{ds\,0}}{V_{dseff}}}, \tag{1}$$

$$I_{ds\,0} \propto \frac{V_{gsteff}\ \mu_{eff} V_{dseff}\left(1-\frac{A_{bulk} V_{dseff}}{2(V_{gsteff}+2V_T)}\right)}{\left(1+\frac{V_{dseff}}{E_{SAT} L_{eff}}\right)}, \tag{2}$$

where I_{ds}, I_{ds0}, R_{ds}, V_{dseff}, V_{gsteff}, A_{bulk}, μ_{eff}, V_T, E_{SAT}, and L_{eff} are the drain current with short-channel effects, drain current of a long channel device, parasitic drain-to-source resistance, effective drain-to-source voltage, effective gate overdrive ($|V_{GS}-V_t|$), parameter to model the bulk charge effect, effective carrier mobility, thermal voltage, electric field at which the carrier drift velocity saturates, and effective channel length, respectively.

Threshold voltage, saturation velocity, and carrier mobility are [6]-[7]

$$NMOS: \quad V_t(T) = V_t(T_0) + \left(KT1 + \frac{KT1L}{L_{eff}} + V_{bseff} KT2\right)\left(\frac{T}{T_0}-1\right), \tag{3}$$

$$PMOS: \quad V_t(T) = V_t(T_0) - \left(KT1 + \frac{KT1L}{L_{eff}} + V_{bseff} KT2\right)\left(\frac{T}{T_0}-1\right), \tag{4}$$

$$V_{SAT}(T) = V_{SAT}(T_0) - AT\left(\frac{T}{T_0}-1\right), \tag{5}$$

$$\mu_{eff}(T) = \left(U_0\left(\frac{T}{T_0}\right)^{U_{te}}\right)\left\{1+\left(\frac{V_{gsteff}+2V_t(T)}{T_{OXE}}\right)^2 U_b(T) + (U_c(T) V_{bseff} + U_a(T))\left(\frac{V_{gsteff}+2V_t(T)}{T_{OXE}}\right)\right\}^{-1}, \tag{6}$$

where V_t, $KT1$, $KT1L$, $KT2$, V_{bseff}, U_0, U_{te}, T_{OXE}, U_a, U_b, U_c, V_{SAT}, AT, T_0, and T are the threshold voltage, temperature coefficient for threshold voltage, channel length dependence of the temperature coefficient for threshold voltage, body-bias coefficient of threshold voltage temperature effect, effective substrate bias voltage, mobility at the reference temperature, mobility temperature exponent, electrical gate-oxide thickness, first order mobility degradation coefficient, second order mobility degradation coefficient, body effect of mobility degradation coefficient, saturation velocity, temperature coefficient of saturation velocity, temperature at which the model parameters are extracted, and the operating temperature, respectively.

As given by (3), (4), (5), and (6), absolute values of threshold voltage, carrier mobility, and saturation velocity degrade as the temperature is increased [6]-[7]. The saturation velocity is typically a weak function of temperature [3]. Threshold voltage degradation with temperature tends to enhance the drain current because of the increase in gate overdrive ($|V_{GS}-V_t|$). Alternatively, degradation in carrier mobility tends to lower the drain current as given by (1) and (2). Effective variation of MOSFET drain current is, therefore, determined by the variation of the dominant device parameter when the temperature fluctuates.

3. DEVICE AND CIRCUIT BEHAVIOR UNDER TEMPERATURE FLUCTUATIONS

Influence of temperature fluctuations on the device and circuit characteristics is evaluated in this section for Berkeley Predictive 65nm CMOS technology [15]. Gate overdrive and carrier mobility variations of n-channel and p-channel devices due to temperature fluctuations at the nominal supply voltage are listed in Table I. Variation of the drain current (I_{DS}) of NMOS and PMOS transistors with supply voltage (V_{DD}) and temperature is shown in Fig. 1. At the nominal supply voltage (V_{DD} = 1.0V), variations of gate overdrive are smaller as compared to carrier mobility variations when the temperature is increased from 25°C to 125°C. The MOSFET drain current of devices operating at the nominal supply voltage is, therefore, degraded as shown in Fig. 1.

TABLE I
GATE OVERDRIVE AND CARRIER MOBILITY VARIATIONS AT THE NOMINAL SUPPLY VOLTAGE (V_{DD} = 1.0V)

65nm CMOS Technology	Gate Overdrive (V)		Carrier Mobility (x10^{-3} m^2/Vs)	
	PMOS	NMOS	PMOS	NMOS
25°C	-0.78	0.78	2.65	9.80
125°C	-0.82	0.82	1.25	4.84
Variation (%)	4.71	4.71	-52.94	-50.60

Propagation delay variations with temperature for circuits operating at the nominal supply voltage in a 65nm CMOS technology are shown in Fig. 2. Propagation delay of a circuit is a function of the drain current produced by active transistors. The circuit speed at the nominal supply voltage degrades primarily due to the reduction of MOSFET currents following the degradation of carrier mobilities when the temperature is increased. The speed of circuits degrade by up to 54.5% as the temperature is increased from 25°C to 125°C, as shown in Fig. 2.

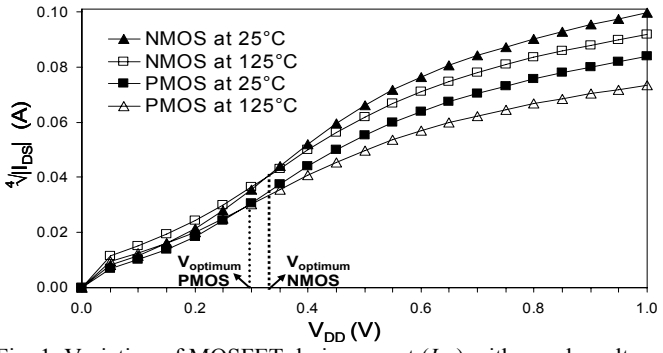

Fig. 1. Variation of MOSFET drain current (I_{DS}) with supply voltage (V_{DD}) and temperature in a 65nm CMOS technology. $|V_{DS}| = |V_{GS}| = V_{DD}$.

4. SUPPLY VOLTAGE OPTIMIZATION

The results presented in Section 3 indicate that operating an integrated circuit at the prescribed nominal supply voltage is not preferable for reliable circuit operation under temperature

fluctuations. A design methodology based on scaling the supply voltage for suppressing the drain current variations due to temperature fluctuations is described in [2], [9], and [14]. In order to counterbalance the variation of carrier mobility, the sensitivity of gate overdrive to temperature fluctuations should be enhanced by lowering the supply voltage [2], [14]. At the optimum supply voltage, the temperature fluctuation induced gate overdrive variation completely compensates the carrier mobility variation [2], [14]. A transistor biased at this optimum supply voltage produces a temperature variation insensitive constant drain current, as illustrated in Fig. 1.

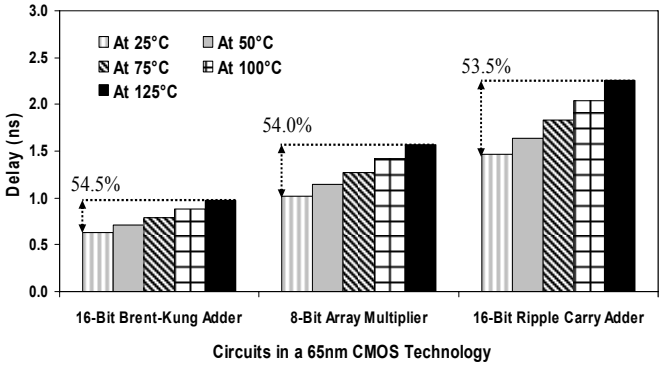

Fig. 2. Percent delay variation with temperature for circuits operating at the nominal supply voltage (V_{DD} = 1.0V).

The optimum supply voltages for test circuits in a 65nm CMOS technology are presented in Fig. 3. Gate overdrive and carrier mobility variations when the temperature fluctuates at the optimum supply voltage are listed in Table II. The degradation of carrier mobility is counterbalanced by an increase in gate overdrive when the temperature is increased at the optimum supply voltage. The MOSFET drain currents and the circuit speed, therefore, become insensitive to temperature fluctuations at the optimum supply voltage, as shown in Fig 3. Circuits display a temperature variation insensitive performance when operated at a supply voltage 67% to 68% lower than the nominal supply voltage (V_{DD} = 1.0V).

As listed in Table I, gate overdrive variations at the nominal supply voltage are equal for n-channel and p-channel devices. Alternatively, temperature fluctuation induced variations in the carrier mobility of a PMOS transistor is higher as compared to an NMOS transistor. The supply voltage should, therefore, be scaled to a lower value in a PMOS device as compared to an NMOS device, to be able to compensate the mobility variations and achieve temperature variation insensitive drain current as shown in Fig. 1. The optimum supply voltage of a CMOS circuit is within the range of the optimum supply voltages of the individual n-channel and p-channel devices, as shown in Figs. 1 and 3.

5. LOW POWER CMOS CIRCUITS

The results presented in Section 4 indicate that there is an optimum supply voltage at which the speed of an integrated circuit is insensitive to temperature fluctuations. The supply voltage that provides temperature variation insensitive circuit performance is lower than the nominal supply voltage. Integrated circuits operating at scaled supply voltages consume low power at the cost of reduced speed. The design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance is, therefore, particularly attractive in low power applications with relaxed speed requirements.

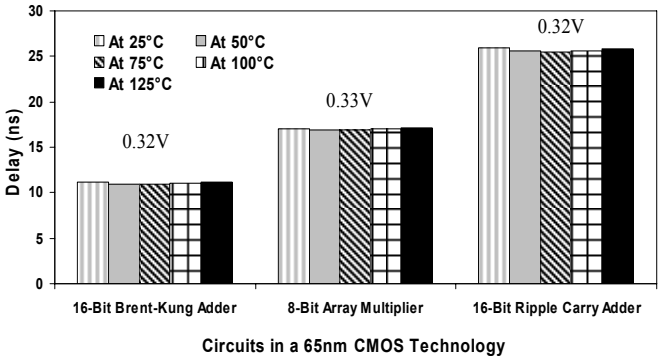

Fig. 3. Optimum supply voltages that achieve temperature variation insensitive speed characteristics.

Low power designs aim at reducing power, power-delay product, and/or energy-delay product [5], [8], [10], [11]. The normalized energy profile of a 16-bit Brent-Kung adder is shown as a function of the supply voltage at 25°C and 125°C in Figs. 4 and 5, respectively. Scaling the supply voltage reduces the dynamic switching energy. Scaling the supply voltage, however, also increases the leakage energy per switching cycle due to the increase in the clock period [10]. The total energy consumption per cycle, therefore, has a minimum as shown in Figs. 4 and 5.

TABLE II
GATE OVERDRIVE AND CARRIER MOBILITY VARIATIONS WITH TEMPERATURE AT THE OPTIMUM SUPPLY VOLTAGE

Temperature (°C)		25	50	75	100	125
NMOS (V_{DD} = 0.34V)	Gate Overdrive (mV)	119	128	138	147	156
	Variation (%)		7.7	15.4	23.0	30.7
	Mobility (x10^{-3} m^2/Vs)	28.9	23.8	20.0	17.1	14.8
	Variation (%)		-17.2	-30.3	-40.5	-48.5
PMOS (V_{DD} = 0.30V)	Gate Overdrive (mV)	-79	-83	-98	-107	-116
	Variation (%)		11.6	23.1	34.7	46.3
	Mobility (x10^{-3} m^2/Vs)	6.7	5.6	4.7	4.1	3.5
	Variation (%)		-16.8	-29.6	-39.7	-47.7

* Percent variations are calculated with respect to the values at 25°C

The supply voltage that provides minimum energy is determined by the relative significance of dynamic switching and leakage energy components. In older technology generations that are less affected by leakage currents, the minimum energy per switching cycle occurs in the subthreshold region ($V_{DD} < |V_t|$) [10]. Supply voltage, threshold voltage, and gate-oxide thickness of MOSFETs are scaled with each new technology generation [13]. Supply voltage scaling reduces the dynamic energy component. Alternatively, the scaling of threshold voltage and gate-oxide thickness increases the

leakage energy component. The dynamic energy to leakage energy ratio is, therefore, reduced with each new technology generation. The supply voltage that minimizes energy consumption is higher for circuits with relatively higher leakage currents [10]. The increased leakage energy per switching cycle shifts the regime where the energy is minimized. For the circuits in this 65nm CMOS technology, the minimum energy consumption is observed in the strong inversion region ($V_{DD} > |V_t| = 0.22V$), as shown in Figs. 4 and 5.

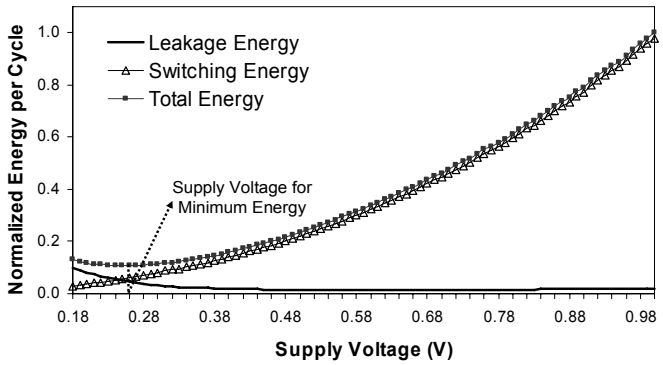

Fig. 4. Normalized total, switching, and leakage energy as a function of the supply voltage at 25°C for a 16-bit Brent-Kung adder.

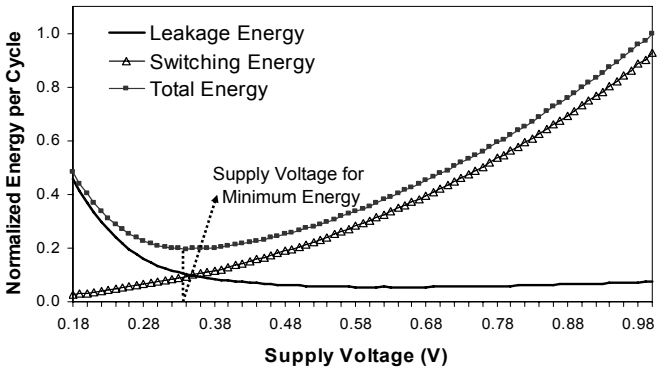

Fig. 5. Normalized total, switching, and leakage energy as a function of the supply voltage at 125°C for a 16-bit Brent-Kung adder.

The normalized energy per switching cycle, propagation delay, and energy-delay product as a function of the supply voltage for a 16-bit Brent-Kung adder at the room temperature (25°C) is shown in Fig. 6. As the supply voltage is reduced, the energy per switching cycle decreases while the propagation delay increases [5]-[8]. The energy-delay product, therefore, has a minimum as shown in Fig. 6.

The energy and propagation delay of circuits operating at the nominal supply voltage are presented in Table III. The energy and propagation delay at the optimum supply voltages providing temperature variation insensitive propagation delay, minimum energy-delay product, and minimum energy are listed in Table IV. The energy and delay at different supply voltages in Table IV are normalized to the energy and propagation delay of the corresponding circuit at the room temperature (25°C) and the nominal supply voltage (V_{DD} = 1.0V). As listed in Table IV, the variation in circuit speed is up to 50% when the temperature is increased from 25°C to 125°C at the supply voltages providing minimum energy-delay product. Similarly, the variation in circuit speed is up to 33% at the supply voltages providing minimum energy. Therefore, similar to the high-speed integrated circuits operating at the nominal supply voltage, low power integrated circuits with deeply scaled supply voltages also require new design methodologies for suppressing the variations in the performance characteristics when the temperature fluctuates.

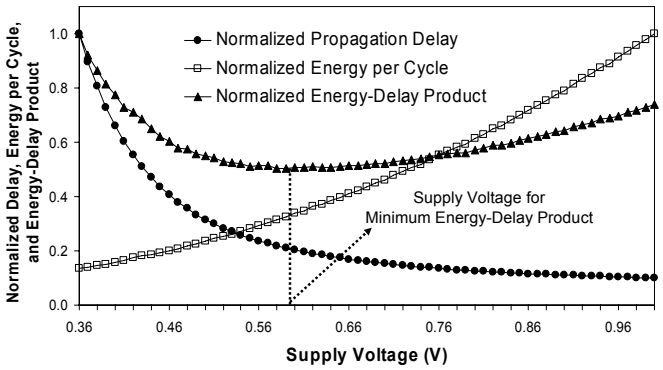

Fig. 6. Normalized energy, delay, and energy-delay product as a function of the supply voltage at the room temperature (25°C) for a 16-bit Brent-Kung adder.

TABLE III
DELAY AND ENERGY PER SWITCHING CYCLE AT THE NOMINAL SUPPLY VOLTAGE

65nm CMOS Technology		Temp (°C)	16-Bit Brent-Kung Adder	8-Bit Array Multiplier	16-Bit Ripple Carry Adder
At the Nominal Supply Voltage (V_{DD} = 1.0V)	Delay (ps)	25	633.30	1015.90	1470.70
		125	978.64	1563.80	2256.95
	Energy (fJ)	25	467.67	676.51	363.23
		125	506.83	852.48	415.84

6. TEMPERATURE VARIATION INSENSITIVE LOW POWER CMOS CIRCUITS

The tradeoffs of operating the circuits at the optimum supply voltages are discussed in this section. The energy and propagation delay characteristics at the supply voltages that yield temperature variation insensitive circuit performance, minimum energy, and minimum energy-delay product are compared.

As listed in Table IV, supply voltages that yield temperature variation insensitive circuit performance and minimum energy are lower than the supply voltages providing minimum energy-delay product. When the circuits are operated at the supply voltages for minimum energy-delay product and minimum energy, the circuit speed is degraded by up to 2.1x and 45.4x, respectively, as compared to the speed at the nominal supply voltage. Similarly, the propagation delay at the temperature variation insensitive optimum supply voltages is up to 17.6x longer than the delay at the nominal supply voltage.

At the supply voltages providing minimum energy-delay product, the energy is 48.3% to 67.5% lower than the energy consumed at the nominal supply voltage (V_{DD} = 1.0V). Similarly, the minimum energy is 64.8% to 89.3% lower than the energy per switching cycle at the nominal supply voltage. At the temperature variation insensitive optimum supply

TABLE IV
NORMALIZED DELAY AND ENERGY AT THE OPTIMUM SUPPLY VOLTAGE AND THE SUPPLY VOLTAGES PROVIDING MINIMUM ENERGY-DELAY PRODUCT AND MINIMUM ENERGY

65nm CMOS Technology	Temp (°C)	Supply Voltage Optimized for Temperature Variation Insensitive Delay			Supply Voltage Optimized for Minimum Energy-Delay Product at 25°C			Supply Voltage Optimized for Minimum Energy-Delay Product at 125°C			Supply Voltage Optimized for Minimum Energy at 25°C			Supply Voltage Optimized for Minimum Energy at 125°C		
		V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*	V_{DD} (V)	Delay	E^*
16-Bit Brent-Kung Adder	25	0.32	17.6	0.12	0.59	2.1	0.32	0.60	2.0	0.34	0.25	45.4	0.11	0.34	12.7	0.13
	125		17.6	0.22		3.1	0.38		3.0	0.39		35.8	0.29		13.8	0.21
8-Bit Array Multiplier	25	0.33	16.8	0.19	0.68	1.7	0.42	0.71	1.6	0.46	0.34	14.8	0.19	0.47	4.3	0.23
	125		16.9	0.57		2.5	0.61		2.4	0.65		15.3	0.55		5.8	0.44
16-Bit Ripple Carry Adder	25	0.32	17.6	0.14	0.63	1.8	0.35	0.63	1.8	0.35	0.31	18.9	0.14	0.41	6.0	0.17
	125		17.6	0.34		2.7	0.46		2.7	0.46		18.5	0.35		7.6	0.30

E^* - Normalized Energy

voltage, the energy is 54.7% to 88.3% lower than the energy at the nominal supply voltage.

Low power integrated circuits optimized for minimum energy and minimum energy-delay product are highly sensitive to temperature fluctuations. Alternatively, integrated circuits with supply voltages optimized for temperature fluctuation insensitive speed characteristics also have drastically reduced energy consumption. Energy efficiency and temperature fluctuation tolerance are therefore simultaneously achieved with the presented supply voltage optimization technique.

7. CONCLUSIONS

A design methodology for temperature variation insensitive low power circuits in a 65nm CMOS technology is presented in this paper. Temperature dependent device parameters that cause variations in MOSFET drain current are identified. When operating at the nominal supply voltage, the speed of circuits degrade by up to 54.5% as the temperature is increased from 25°C to 125°C. Operating an integrated circuit at the prescribed nominal supply voltage is not preferable for reliable circuit operation under temperature fluctuations. Circuits display a temperature variation insensitive performance when operated at a supply voltage 67% to 68% lower than the nominal supply voltage (V_{DD} = 1.0V) in a 65nm CMOS technology.

Integrated circuits operating at scaled supply voltages consume low power at the cost of reduced performance. The design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance is, therefore, particularly attractive in low power applications with relaxed speed requirements. The optimum supply voltages are similar for a diverse set of circuits in a 65nm CMOS technology. The proposed technique of operating large scale designs at an optimum supply voltage for simultaneously achieving energy efficiency and temperature variation insensitive speed is demonstrated to be feasible.

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