Leakage Current Starved Domino Logic

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ABSTRACT

A new circuit technique based on a single PMOS sleep transistor and a dual threshold voltage CMOS technology is proposed in this paper for simultaneously reducing subthreshold and gate oxide leakage currents in idle domino logic circuits. In the sleep mode, the output inverter and keeper transistor of a domino gate are disconnected from the power supply by turning off a high threshold voltage sleep switch. The dynamic and output nodes are discharged by the initially high subthreshold and gate oxide leakage currents produced by the NMOS transistors in the pull-down network, output inverter, and fan-out gates. After the node voltages settle, the circuit is placed into a low subthreshold and gate oxide leakage state. The effectiveness of the circuit technique for suppressing leakage current is verified under significant fluctuations of channel length, gate oxide thickness, and channel doping concentration due to process variations. The proposed circuit technique lowers the total leakage power by 67.7% to 98.8% as compared to standard dual threshold voltage domino logic circuits. Similarly, an 11.7% to 84.1% reduction in total leakage power is observed as compared to a previous sleep switch scheme in a 45nm CMOS technology.

Categories and Subject Descriptors

B.7.1 **[Integrated Circuit]**: Types and Design Styles – VLSI (very large scale integration), advanced technologies.

General Terms

Design, performance.

1. INTRODUCTION

CMOS technology scaling requires reducing the supply and threshold voltages. Lowering of threshold voltages leads to an exponential increase in subthreshold leakage current. Several circuit techniques based on multiple threshold voltage (multiple-V_t) CMOS technologies are described in the literature for reducing the subthreshold leakage current [1]-[2], [5]. However, effect of these multiple-V_t CMOS circuit techniques on the gate oxide leakage current characteristics has not been explored until recently.

Under normal bias conditions of a typical deep sub-micrometer MOSFET (oxide voltage < tunneling barrier height), gate oxide leakage current (I_{gate}) is caused by direct tunneling of electrons and holes through thin gate insulator layer [11]. Tunneling current density increases dramatically with the scaling of gate oxide thickness (t_{ox}) in each new technology generation. A comparison of gate oxide and subthreshold leakage currents of an NMOS transistor at two different die temperatures is shown in Fig. 1, in a 45nm CMOS technology. At 110 ºC, the subthreshold leakage current ($I_{subthreshold}$) is 6.7 × higher than I_{gate} (operating at the nominal supply voltage 0.8V) as illustrated in Fig. 1. Alternatively, at the room temperature, I_{gate} is 2.5 × higher than $I_{subthreshold}$. As aggressive scaling of t_{ox} continues, gate dielectric tunneling will soon become a primary leakage mechanism. Particularly at low die temperatures during long idle periods, most of the power consumption could occur due to the direct tunneling of carriers through thin gate oxides. New circuit techniques aimed at reducing both subthreshold and gate oxide leakage currents are, therefore, highly desirable.

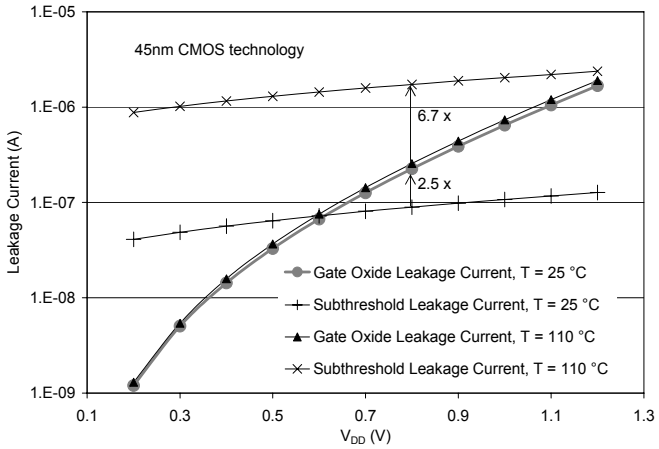

Fig. 1. Comparison of subthreshold and gate oxide leakage currents produced by an NMOS transistor for various supply voltages at two different die temperatures. $I_{subthreshold}$: $V_{GS} = 0$ and $V_{DS} = V_{DD}$. I_{gate}: $V_{GS} = V_{GD} = V_{GB} = V_{DD}$.

In this paper, a new circuit technique is proposed to reduce both subthreshold and gate oxide leakage currents in idle domino logic circuits. A single PMOS sleep transistor is utilized along with a dual threshold voltage (dual-V_t) CMOS technology and clock gating to place an idle domino circuit into a low subthreshold and gate oxide leakage current state. The proposed technique reduces the total leakage power by 67.7% to 98.8% as compared to standard dual-V_t domino logic circuits.

The paper is organized as follows. Leakage current characteristics of domino circuits are described in Section 2. The new circuit technique to reduce total leakage power is presented in Section 3. Simulation results at the nominal design corner are given in Section 4. Process parameter variations are addressed in Section 5. Some conclusions are offered in Section 6.

2. LEAKAGE CURRENT CHARACTERISTICS OF DYNAMIC CMOS CIRCUITS

Leakage current characteristics of dynamic CMOS circuits are explored in this section. Subthreshold and gate oxide leakage currents produced by NMOS and PMOS transistors are compared in Section 2.1. Leakage current characteristics of previously published sleep switch dual-V_t domino logic circuit techniques in the literature are discussed in Sections 2.2 and 2.3.

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2.1 Comparison of Leakage Currents in N-Channel and P-Channel Devices

Subthreshold and gate oxide leakage currents produced by NMOS and PMOS transistors are illustrated in Fig. 2. I_{gate} has four components as shown in Fig. 2a: gate-to-channel tunneling current (I_{gc}), gate-to-drain tunneling current (I_{gd}), gate-to-source tunneling current (I_{gs}), and gate-to-body tunneling current (I_{gb}). Tunneling current from the gate terminal to the conducting channel (I_{gc}) is shared between the source and drain terminals [6]. I_{gs} and I_{gd} are edge tunneling currents through the gate-to-source and gate-to-drain overlap areas, respectively. I_{gb} is typically several orders of magnitude smaller than the other three components of gate tunneling current.

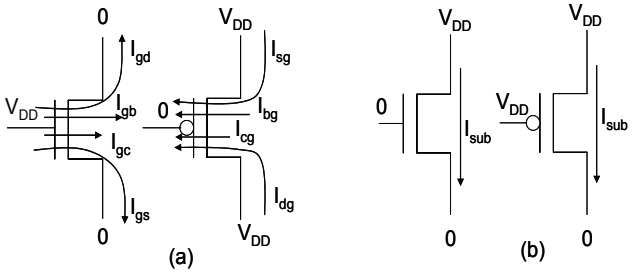

Fig. 2. Maximum gate oxide and subthreshold leakage current states in NMOS and PMOS transistors. (a) Maximum gate oxide leakage current state. (b) Maximum subthreshold leakage current state.

Highest gate oxide leakage current is observed when a transistor operates in active region with the maximum voltage difference across the gate-to-source and the gate-to-drain terminals, as illustrated in Fig. 2a. Alternatively, highest subthreshold leakage current is observed when a cut-off transistor is biased with the maximum voltage difference between the source and drain terminals, as shown in Fig. 2b.

Table 1. Normalized $I_{subthreshold}$ and I_{gate} of low-V_t and high-V_t transistors at two different die temperatures

	NMOS Transistor		PMOS Transistor	
	Low-V_t	High-V_t	Low-V_t	High-V_t
$I_{subthreshold}$ (110 ºC)	31.5	1.1	22.7	1.0
I_{gate} (110 ºC)	4.7	3.5	0.1	0.1
$I_{subthreshold}$ (25 ºC)	63.0	0.8	52.8	1.0
I_{gate} (25 ºC)	159.1	124.0	5.3	5.3

*** Transistor width = 1 µm. Transistor length = 45 nm. |Low-V_t| = 0.22 V. |High-V_t| = 0.35 V. V_{DD} = 0.8 V. $I_{subthreshold}$: V_{GS} = 0 and $|V_{DS}| = V_{DD}$. I_{gate}: $|V_{GS}| = |V_{GD}| = |V_{GB}| = V_{DD}$. For each temperature, currents are normalized to the subthreshold leakage current produced by high-V_t PMOS transistor.**

A comparison of the normalized subthreshold and gate oxide leakage currents of low threshold voltage (low-V_t) and high threshold voltage (high-V_t) transistors in a 45nm dual-V_t CMOS technology is listed in Table 1. The data are measured at the upper and lower extremes of a typical microprocessor die temperature spectrum.

The I_{gate} produced by a low-V_t NMOS transistor is 47 × and 30 × higher than the I_{gate} produced by a low-V_t PMOS transistor at 110 ºC and 25 ºC, respectively, as listed in Table 1. In a technology utilizing silicon dioxide as the gate dielectric material, the tunneling barrier for holes is much higher than the tunneling barrier for electrons. The I_{gate} for a PMOS device is, therefore, significantly lower as compared to an NMOS device with the same physical dimensions (width, length, and t_{ox}) and the same voltage difference across the gate insulator.

2.2 Dual-V_t Domino Logic

Employing dual-V_t transistors for subthreshold leakage current reduction in domino logic circuits was first proposed by Kao [1]. The critical signal transitions that determine the delay of a domino logic circuit occur along the evaluation path. In a dual-V_t domino circuit, therefore, all of the transistors that can be activated during the evaluation phase have a low-V_t. Alternatively, the precharge phase transitions are not critical for the performance of a domino logic circuit. Therefore, those transistors that are active during the precharge phase have a high-V_t [5].

Gating all of the inputs of the first stage of a domino pipeline is proposed in [1] to place the idle domino circuits into a low leakage state. Additional gates are employed at each input of the first stage domino gates in a multiple stage domino logic circuit with this technique, as shown in Fig. 3. The clock is gated high, turning off the high-V_t precharge transistor when a domino logic circuit is idle. The sleep signal transitions to high activating the pull-down network transistors regardless of the actual input vector. The dynamic nodes of the first stage domino gates are discharged. After forcing the first stage domino gates to evaluate and discharge, the domino gates of the subsequent stages in the pipeline also evaluate and discharge. The sleeping process is similar to dominos tipping over with each stage triggering the next into a sleep state. After the node voltages settle, all of the high-V_t transistors are cut-off, thereby reducing the subthreshold leakage current as compared to a low-V_t circuit [3].

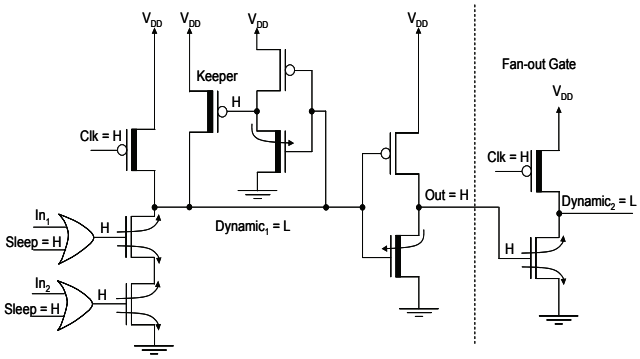

Fig. 3. A two-input dual-V_t domino AND gate with inputs gated high in sleep mode. The most significant components of gate oxide leakage current in the sleep mode are illustrated with arrows. H: high. L: low. High-V_t transistors are represented by a thick line in the channel region.

Similar subthreshold leakage current reduction techniques based on discharging and charging the dynamic and output nodes, respectively, of all of the domino gates in a dynamic circuit have been proposed in [1]-[2]. High output of an idle domino gate, however, places the fan-out domino circuits into the highest gate oxide leakage current state, as illustrated in Fig. 3. The techniques proposed in [1]-[2] and [5], therefore, increase gate oxide leakage current while reducing subthreshold leakage current. In the sub-65 nm CMOS technologies, significant increase in gate oxide leakage

current could negate the subthreshold leakage current reduction provided by these techniques, thereby increasing the total leakage energy consumed by an idle domino circuit.

2.3 NMOS Sleep Switch Dual-V_t Domino Logic

For an idle dual-V_t domino gate with a high input vector, bulk of the gate tunneling current is produced by the low-V_t NMOS transistors in the pull-down network. Alternatively, subthreshold leakage current is produced by the high-V_t transistors. As listed in Table 1, the I_{gate} of a low-V_t NMOS transistor is 4.7 × and 159.1 × higher than the $I_{subthreshold}$ of a high-V_t PMOS transistor at the high and low die temperatures, respectively. Similarly, the I_{gate} of a low-V_t NMOS transistor is 4.3 × and 198.9 × higher than the $I_{subthreshold}$ of a high-V_t NMOS transistor at the high and low die temperatures, respectively. Gate tunneling is, therefore, the dominant leakage mechanism in a dual-V_t domino gate at both high and low die temperatures provided that the inputs are maintained high in the idle mode.

In addition to setting the dynamic node voltage low for reducing subthreshold leakage current, the output node of a domino logic circuit should also be placed into a low voltage state in order to suppress the gate oxide leakage currents in the fan-out gates. A technique to force both the dynamic and the output nodes of a domino logic circuit into a low voltage state in standby mode is proposed in [6]. Two high-V_t NMOS sleep transistors N1 and N2 are placed at the dynamic and output nodes, respectively, as illustrated in Fig. 4.

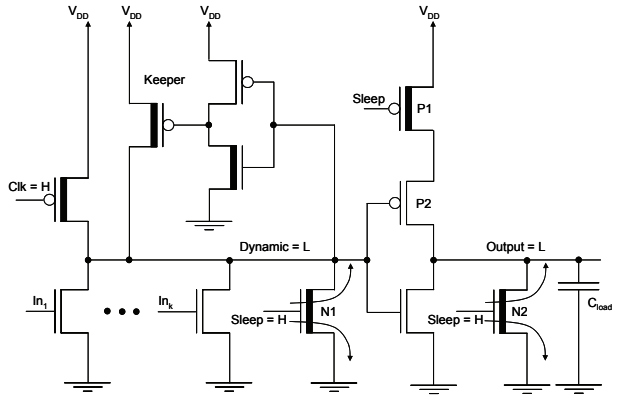

Fig. 4. A k-input NMOS sleep switch dual-V_t domino OR gate in sleep mode. Gate oxide leakage currents produced by the sleep transistors are illustrated with arrows. H: high. L: low. High-V_t transistors are represented by a thick line in the channel region.

In the standby mode, clock is gated high. The sleep signal is set high turning on N1 and N2. The dynamic and output nodes are discharged through N1 and N2, respectively. P1 is cut-off to avoid a static DC current path through P2 and N2. After the dynamic and output nodes are discharged, the two NMOS sleep transistors (N1 and N2) are both in the maximum gate oxide leakage current state (see Fig. 4). Sleep transistors (N1, N2, and P1) are required within every domino gate in a dynamic circuit designed with the technique presented in [6]. Gate oxide leakage current overhead of the NMOS sleep transistors, therefore, imposes a serious limitation to the leakage current reduction that can be provided by this technique. Furthermore, an extra inverter is required to control the operation of the keeper transistor in every domino gate, thereby increasing the area and active mode power overhead with this technique.

3. CURRENT STARVED DUAL-V_t DOMINO LOGIC

A new circuit technique with enhanced effectiveness to simultaneously reduce subthreshold and gate oxide leakage currents in domino logic circuits is proposed in this paper. Only one PMOS sleep transistor is employed in each domino gate in order to reduce the gate oxide leakage current, sleep mode energy, and area overheads with the new circuit technique. The proposed circuit technique is illustrated in Fig. 5. A high-V_t PMOS sleep transistor (P1) is employed in order to cut-off the V_{DD} connection to the output inverter and the keeper during the sleep mode.

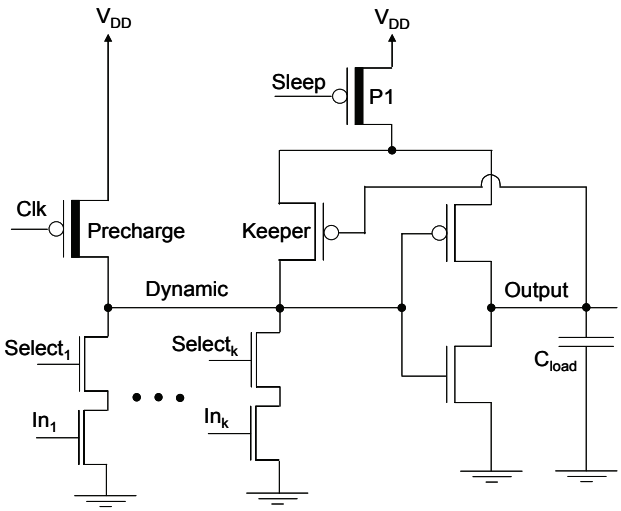

Fig. 5. A k-bit current starved dual-V_t domino multiplexer with a high-V_t PMOS sleep transistor (P1). High-V_t transistors are represented by a thick line in the channel region.

In the active mode, the sleep signal is set low. P1 is turned on. The domino gate operates similar to a standard dual-V_t domino circuit. In the standby mode, the clock is gated high, turning off the high-V_t precharge transistor. The sleep signal is set high, cutting off P1. Provided that the dynamic node is at a high voltage stage at the beginning of idle mode, dynamic node is eventually discharged by the initially high sub-threshold leakage currents of the low-V_t NMOS transistors in the pull-down network. Alternatively, provided that the output node is at a high voltage state at the beginning of idle mode, output node is eventually discharged by the initially high subthreshold leakage current of low-V_t NMOS transistor in the output inverter and the gate tunneling current of NMOS transistors in the pull-down networks of fan-out gates. In steady state, the dynamic and output nodes are maintained at a low voltage state due to the significantly higher subthreshold resistance of the high-V_t precharge and sleep transistors as compared to the low-V_t pull-down transistors. After the node voltages settle to a steady state, voltages across the gate insulating layers of all of the critical NMOS transistors are suppressed, thereby lowering the gate oxide leakage current. Similarly, the high-V_t precharge and sleep transistors are strongly cut-off, significantly reducing subthreshold leakage current with the current starved dual-V_t domino logic circuit technique.

4. SIMULATION RESULTS

BSIM4 device models are used in this paper for an accurate estimation of gate oxide leakage current [4]. Following circuits are simulated in a 45nm CMOS technology ($V_{tnlow} = |V_{tplow}| = 0.22V$, $V_{tnhigh} = |V_{tphigh}| = 0.35V$, and $V_{DD} = 0.8V$): 2-input domino AND gate (AND2), 2-input, 4-input, and 8-input domino OR gates (OR2, OR4, and OR8, respectively), and 16-bit domino multiplexer (MUX16). All of the circuits (other than MUX16) are composed of three stages. Each gate drives a fan-out of four. The domino gates in the first stage are footed while the gates in the second and third stages are footless. All of the circuits are designed with the following three techniques: standard dual-V_t domino (dual-V_t), the technique presented in [6] (dual-V_t-NMOS), and the leakage current starved sleep switch circuit technique proposed in this paper (current-starved). A 3 GHz clock is applied to the circuits. To have a reasonable comparison, the circuits are sized to have a similar worst-case propagation delay with each technique. Sleep mode data are measured at both 110 °C and 25 °C assuming short and long idle periods, respectively. Active mode data are measured at 110 °C.

4.1 Active Mode Power Consumption

Active power consumption of the domino circuits is shown in Fig. 6. In dual-V_t-NMOS and current-starved circuits, two PMOS transistors are placed in series in the pull-up path of the output inverter. Furthermore, P1 (Figs. 4 and 5) has a high-V_t. Driving capability of the output inverter is, therefore, degraded. Physical size of PMOS transistors in the output inverters of current-starved and dual-V_t-NMOS circuits is increased to provide an evaluation delay similar to standard dual-V_t circuits.

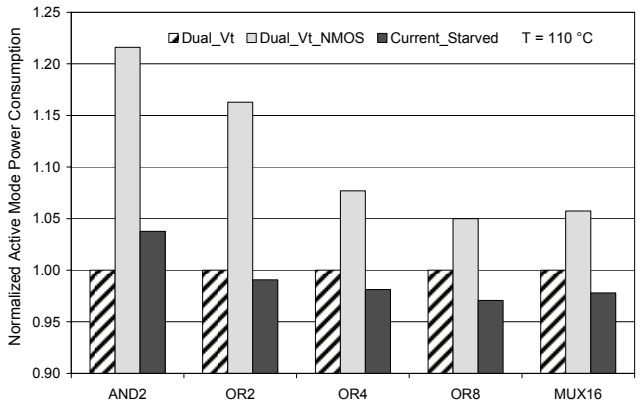

Fig. 6. Comparison of active mode power consumption with the three domino circuit techniques. For each circuit, power consumption is normalized to the power consumed by standard dual-V_t technique.

For dual-V_t-NMOS circuits, parasitic capacitance at the dynamic and output nodes is increased due to the additional parasitic capacitance introduced by the sleep transistors and the extra inverter. Therefore, as shown in Fig. 6, active mode power consumption of the dual-V_t-NMOS circuits is higher than the standard dual-V_t circuits. Alternatively, in the proposed current-starved circuits, there is only one sleep transistor (P1) which is isolated from the dynamic and output nodes. Furthermore, NMOS transistor in the output inverter of a current-starved circuit can be sized smaller since this transistor has a lower threshold voltage as compared to a standard dual-V_t circuit. The active mode power characteristics of current-starved circuits are determined by the tradeoff between the increased size of PMOS transistor and the decreased size of NMOS transistor in the output inverter. The active mode power consumption of most of the current-starved circuits is reduced (by up to 3%, OR8) as compared to standard dual-V_t circuits, as shown in Fig. 6.

The dual-V_t-NMOS technique increases the active mode power consumption by 5% (OR8) to 22% (AND2) as compared to the standard dual-V_t domino circuits. Current-starved circuits reduce the active power consumption by 8.5% (OR2) to 9.3% (MUX16) as compared to dual-V_t-NMOS circuits due to the simplicity of the proposed sleep scheme.

4.2 Leakage Power Consumption at 110 °C

In this section, the circuits are assumed to be operating at a worst case high temperature of 110 °C before the beginning of idle mode. Furthermore, it is assumed that the idle mode is short. Total leakage power consumption of the domino circuits at 110 °C (assuming the die temperature does not significantly change during the short idle period) is shown in Fig. 7.

As described in Section 3, the dynamic and output nodes of an idle current-starved circuit are eventually discharged to a low voltage level by the initially high subthreshold and gate oxide leakage currents. Steady-state dynamic and output node voltages in the current-starved domino circuits are listed in Table 2.

Table 2. Steady-state dynamic and output node voltages in current-starved circuits

Node	AND2	OR2	OR4	OR8	MUX16
Dynamic (mV)	7.3	3.3	2.5	1.4	3.2
Output (mV)	12.5	4.9	15.2	10.9	19.5

Subthreshold leakage current produced by a standard domino logic circuit strongly depends on the dynamic and output node voltages [3]. Two input conditions are simulated to evaluate the leakage current in the sleep mode with the standard dual-V_t technique. First condition assumes that all of the inputs applied to the first stage gates are low (high dynamic node voltage state). Second condition assumes that all of the inputs applied to the first stage gates are gated high (low dynamic node voltage state) as proposed in [1].

For an idle standard dual-V_t domino gate, a high input vector turns off the high-V_t transistors, thereby reducing the subthreshold leakage current. However, a high input vector also places the pull-down network into the maximum gate insulator tunneling current state. Since the I_{gate} of NMOS transistors is higher than the $I_{subthreshold}$ of high-V_t transistors at 110 °C (See Table 1), the gate tunneling currents produced by the pull-down network transistors dominate the total leakage power consumption of an idle dual-V_t domino gate driven with high inputs even at this worst case high temperature.

The current-starved and dual-V_t-NMOS circuit techniques discharge both the dynamic and output nodes of an idle domino gate, thereby significantly reducing the subthreshold and gate oxide leakage currents as compared to standard dual-V_t domino circuits. In a dual-V_t-NMOS gate, however, two NMOS sleep transistors are employed at the dynamic and output nodes. After dynamic and output nodes are discharged by activating these sleep transistors, both NMOS sleep transistors operate at the maximum gate oxide leakage current state throughout the idle mode ($V_{gs} = V_{gd} = V_{DD}$).

Alternatively, in a current-starved domino gate, the only sleep transistor is a high-V_t PMOS transistor in series with the output inverter and keeper. Removing the NMOS sleep transistors at the dynamic and output nodes and employing only one inverter per gate reduces the leakage and active mode power overhead of current-starved circuits.

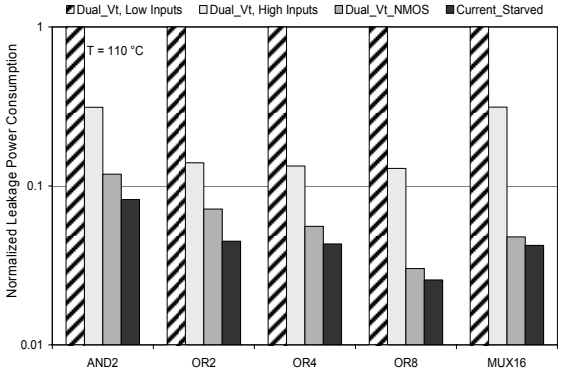

Fig. 7. Comparison of total leakage power consumed by domino circuits with the three circuit techniques at 110 °C. For each circuit, leakage power is normalized to the leakage power of standard dual-V_t technique with low inputs.

The current-starved technique reduces the total leakage power by 67.7% (OR4) to 86.5% (MUX16) as compared to the standard dual-V_t circuits with a high input vector, as shown in Fig. 7. Standard dual-V_t circuits consume more leakage power with a low input vector since the subthreshold leakage current is produced by the low-V_t transistors when the inputs are low. The current-starved technique reduces the total leakage power by 91.8% (AND2) to 97.4% (OR8) as compared to the standard dual-V_t circuits with a low input vector. Furthermore, the current-starved technique reduces the leakage power consumption by 11.7% (MUX16) to 37.2% (OR2) as compared to the dual-V_t-NMOS technique due to the high gate tunneling current overhead of the NMOS sleep switches and the leakage overhead of the extra inverter with the dual-V_t-NMOS technique.

4.3 Leakage Power Consumption at 25 °C

In this section, idle mode is assumed to be long. The die temperature is assumed to be cooled to the ambient room temperature during long idle periods. The total leakage power consumption of the domino circuits at 25 °C is compared in Fig. 8. At the room temperature, gate tunneling is the dominant leakage mechanism (See Table 1). Contrary to the previous low leakage circuit techniques [1]-[2], maintaining inputs low is preferable for reducing the total leakage power consumption of the standard dual-V_t domino circuits (except OR2) as shown in Fig. 8. This result indicates a dramatic change in the leakage power characteristics of standard domino logic circuits due to the significant gate oxide tunneling through thin gate insulator layers in this deeply scaled nanometer CMOS technology [7]-[8].

The current-starved technique reduces the total leakage power by 88.1% (MUX16) to 98.6% (OR8) as compared to the standard dual-V_t circuits driven with low inputs, as shown in Fig. 8. For a higher fan-in, the leakage power savings provided by the current-starved technique is enhanced (OR2: 97.8% versus OR8: 98.6%). The standard dual-V_t circuits consume more leakage power with a high input vector due to the significant gate oxide leakage current produced by the NMOS transistors in the pull-down network when the inputs are gated high. The current-starved technique reduces the total leakage power by 94.1% (MUX16) to 98.8% (OR8) as compared to standard dual-V_t circuits driven with high inputs.

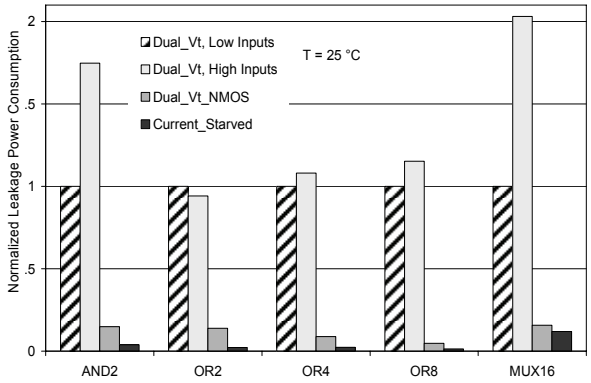

Fig. 8. Comparison of total leakage power consumed by domino circuits with the three circuit techniques at 25 °C. For each circuit, leakage power is normalized to the leakage power of standard dual-V_t technique with low inputs.

The dual-V_t-NMOS technique suppresses the gate tunneling current of the pull-down network transistors in the fan-out gates by discharging the output node. Similarly, the subthreshold leakage current is reduced by cutting-off all of the high-V_t transistors (other than N1 and N2) in the sleep mode. However, all of the NMOS sleep transistors (required within every domino gate) are placed into the maximum gate oxide leakage current state with the dual-V_t-NMOS technique. The NMOS sleep switches added to the dual-V_t-NMOS circuits, therefore, introduce a significant gate oxide leakage current overhead. Furthermore, the extra inverter required to control the keeper transistor causes additional leakage power consumption.

The proposed current-starved sleep scheme effectively eliminates the gate oxide leakage overhead introduced by the sleep transistors. Furthermore, the output inverter can be used to drive both the keeper and the fan-out gates with the proposed technique as shown in Fig. 5. The current-starved technique reduces the total leakage power by 24.3% (MUX16) to 84.1% (OR2) as compared to the dual-V_t-NMOS technique, as shown in Fig. 8.

5. PROCESS PARAMETER VARIATIONS

Random and systematic fluctuations in channel length, doping concentration, and gate oxide thickness cause variations in MOSFET characteristics. The subthreshold and gate oxide leakage currents vary with the fluctuations of threshold voltage and gate oxide thickness, inducing variations in the leakage power consumption of CMOS circuits [9]-[10].

In this section, leakage power variations of domino logic circuits due to process variations in gate length (L_{gate}), channel doping concentration (N_{ch}), and t_{ox} are evaluated. L_{gate}, N_{ch}, and t_{ox} are assumed to have normal Gaussian statistical distributions. Each parameter is assumed to have a three sigma (3σ) variation of 10% [9]. 10,000 Monte Carlo simulations are run to evaluate the leakage power distribution due to process parameter variations.

The leakage power characteristics of domino AND gates with the current-starved and dual-V_t-NMOS techniques at 110 °C and 25 °C are shown in Fig. 9. The average and standard deviations (SD) of the leakage power of current-starved and dual-V_t-NMOS domino circuits are listed in Table 3.

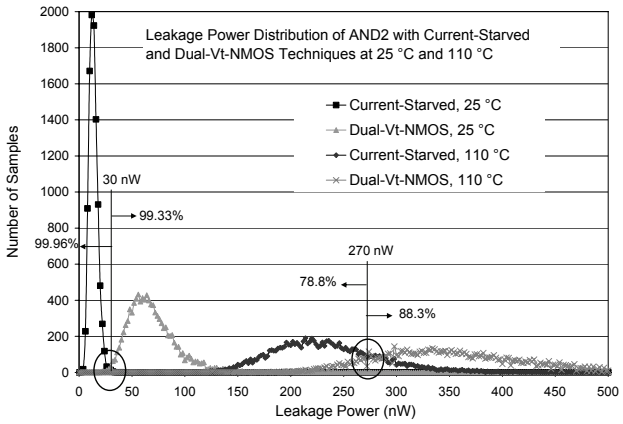

Fig. 9. Comparison of the leakage power distributions of 2-input dual-V_t domino AND gates due to process parameter variations at 110 ºC and 25 ºC.

The leakage power distribution curves of the current-starved and dual-V_t-NMOS AND gates cross at 270 nW at 110 ºC, as shown in Fig. 9. Leakage power consumption of 78.8% of the samples with the current-starved technique is lower than 270 nW. Alternatively, 88.3% of the samples with the dual-V_t-NMOS technique consume leakage power higher than 270 nW.

At the room temperature, the leakage power distribution curves of the current-starved and dual-V_t-NMOS gates intersect at 30 nW, as shown in Fig. 9. Leakage power consumption of 99.96% of the samples with the current-starved technique is lower than 30 nW. Alternatively, 99.33% of the samples with the dual-V_t-NMOS technique consume leakage power higher than 30 nW. These results indicate that the current-starved technique is highly effective to reduce the total leakage power consumption even under significant process variations.

Table 3. Average and standard deviation of leakage power (nW) of current-starved and dual-V_t-NMOS circuits

Average/SD	Current-Starved		Dual-V_t-NMOS	
	110 °C	25 °C	110 °C	25 °C
AND2	234/50	14/4	354/74	69/22
OR2	165/38	17/7	261/54	59/20
OR4	338/78	35/15	385/82	73/24
OR8	360/84	39/17	423/91	77/26
MUX16	1040/245	367/126	1180/259	503/182

As listed in Table 3, the reduction in average power consumption obtained by Monte Carlo simulations is similar to the leakage reduction provided at the nominal design corner (see Figs. 7 and 8). The current-starved circuits reduce the average total leakage power by up to 35% and 80% at 110 °C and 25 °C, respectively, as compared to dual-V_t-NMOS circuits under significant process parameter variations.

6. CONCLUSIONS

In the sub-65 nm CMOS technologies, both subthreshold and gate dielectric leakage currents need to be suppressed for reducing standby power consumption. A circuit technique employing a single sleep transistor and a dual-V_t CMOS technology is presented in this paper for simultaneously reducing subthreshold and gate oxide leakage currents in domino logic circuits.

The proposed current starved domino circuit technique exploits the initially high subthreshold and gate oxide leakage currents of low-V_t pull-down transistors for placing an idle domino logic circuit into an ultimately low leakage state. In the sleep mode, the high-V_t precharge and sleep transistors are strongly cut-off, reducing the subthreshold leakage current. Furthermore, the gate dielectric tunneling currents in the fan-out gates are suppressed by discharging the output nodes of the domino gates.

The circuit technique reduces the total leakage power by 67.7% to 98.8% as compared to the standard dual-V_t domino circuits in the sleep mode. Furthermore, by employing only a single high-V_t PMOS sleep transistor per gate, the presented circuit technique reduces the total leakage power by 11.7% to 84.1% as compared to a previously published technique based on NMOS sleep switches. The effectiveness of the circuit technique for suppressing leakage current is verified under significant process variations. The current-starved circuits reduce the average total leakage power by up to 37.2% and 84.1% at 110 °C and 25 °C, respectively, as compared to dual-V_t-NMOS circuits.

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