A Design Methodology for Temperature Variation Insensitive Low Power Circuits

Ranjith Kumar and Volkan Kursun

Department of Electrical and Computer Engineering
University of Wisconsin – Madison
Madison, Wisconsin 53706-1691

Abstract

Operating an integrated circuit at the prescribed nominal supply voltage is not preferable for reliable circuit operation under temperature fluctuations. A design methodology based on optimizing the supply voltage for temperature variation insensitive circuit performance is presented in this paper. Circuits display temperature variation insensitive delay characteristics when operated at a supply voltage 45% to 53% lower than the nominal supply voltage (V_{DD} = 1.8V) in a 180nm CMOS technology. Integrated circuits operating at scaled supply voltages consume low power at the cost of reduced speed. The proposed design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance is, therefore, particularly attractive in low power applications with relaxed speed requirements. The energy, delay, and energy-delay product (EDP) are compared at the supply voltages that yield temperature variation insensitive circuit performance and minimum energy-delay product. Results indicate that low-power integrated circuits can also be made insensitive to temperature fluctuations with a modest amount of increase in energy-delay product.

Categories and Subject Descriptors
B.7.1 [Integrated Circuits]: Types and Design Styles.

General Terms: Design, reliability, performance.

1. INTRODUCTION

Process and environment parameter variations are posing greater challenges in the design of reliable integrated circuits in scaled CMOS technologies. Variations can be categorized into die-to-die variations and within-die variations. Die-to-die fluctuations affect every element in an integrated circuit similarly. Alternatively, within-die variations cause a non-uniformity of physical characteristics among the devices in an integrated circuit. The accuracy of estimating the variations relates to the manufacturing cost of an integrated circuit. An overestimation of variations results in a conservative design with increased design effort, thereby delaying the time-to-market and degrading performance. Alternatively, an underestimation of variations compromises reliability and functionality, thereby degrading yield. Increasing within-die parameter fluctuations and the complexity in estimating the variations require new design methodologies for suppressing the effects of process and environment parameter fluctuations in future technology generations.

Because of the imbalanced utilization and diversity of circuitry at different sections of an integrated circuit, temperature can vary significantly from one die area to another [1]. Furthermore, environmental temperature fluctuations can cause significant variations in die temperature. For example, electronic systems mounted on the automobile engines operate at a temperature range from -40°C to 150°C [12]. Temperature variations affect the device characteristics of MOSFETs thereby varying the performance of integrated circuits.

Propagation delay of a circuit is a function of the drain current produced by active transistors. Performance of an integrated circuit under temperature fluctuations is determined by a set of device parameters. Temperature fluctuations alter threshold voltage, carrier mobility, and saturation velocity of a MOSFET [3]. Temperature fluctuation induced variations in individual device parameters have unique effects on MOSFET drain current. The dominant parameter that determines circuit speed varies with the device/circuit bias conditions such as supply voltage and temperature. Variation of the drain current (I_{DS}) of NMOS and PMOS transistors with supply voltage (V_{DD}) and temperature in a 180nm CMOS technology is shown in Fig. 1. At higher supply voltages, the drain saturation current of a MOSFET degrades when the temperature is increased. Alternatively, provided that the supply voltage is low, MOSFET drain current increases with temperature, indicating a change in the dominant device parameter [2]-[4].

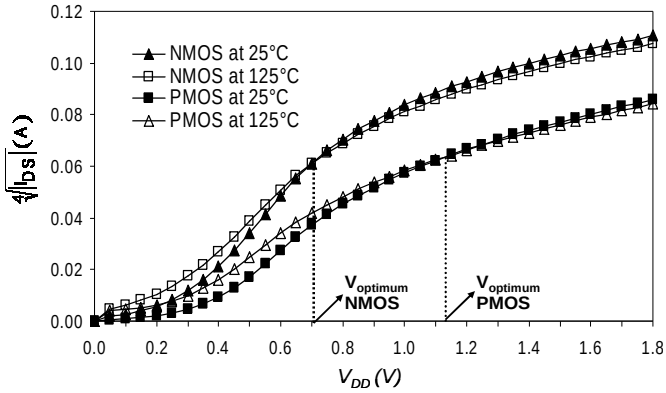

Fig. 1. Variation of MOSFET drain current (I_{DS}) with supply voltage (V_{DD}) and temperature in a 180nm CMOS technology. $|V_{DS}| = |V_{GS}| = V_{DD}$.

There exists a bias voltage for which device parameter variations counterbalance each other's effect on MOSFET current when the temperature fluctuates [2], [4], [9], [13]. The optimum supply voltages for temperature variation insensitive circuit performance are lower than the nominal supply voltage (V_{DD} = 1.8V) in a 180nm CMOS technology [2]. Integrated circuits operating at scaled supply voltages consume low power at the cost of reduced speed. The design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance is, therefore, particularly

This research was supported in part by a grant from the Wisconsin Alumni Research Foundation (WARF).

GLSVLSI'06, April 30–May 2, 2006, Philadelphia, Pennsylvania, USA.

attractive in low power applications with relaxed speed requirements. In this paper, the supply voltages that achieve minimum energy-delay product at two different temperatures are identified for circuits in a 180nm CMOS technology. The energy, delay, and energy-delay product (EDP) are compared at the supply voltages that yield temperature variation insensitive circuit performance and minimum energy-delay product. The tradeoffs in the supply voltage optimization process are presented.

The paper is organized as follows. The influence of temperature dependent device parameters on the drain current of a MOSFET is analyzed in Section 2. Effect of temperature fluctuations on the device and circuit characteristics in a 180nm CMOS technology is examined in Section 3. The optimum supply voltages for temperature variation insensitive circuit performance are presented in Section 4. The supply voltages that yield minimum energy-delay product are identified in Section 5. The tradeoffs of operating the circuits at the supply voltages providing temperature variation insensitive circuit speed are discussed in Section 6. Finally, some conclusions are given in Section 7.

2. FACTORS INFLUENCING MOSFET DRAIN CURRENT UNDER TEMPERATURE FLUCTUATIONS

Device parameters that are affected by temperature fluctuations, causing variations in drain current produced by a MOSFET, are identified in this section. BSIM3 MOSFET current equations are used for an accurate characterization of drain current in deeply scaled nanometer devices. The drain current of a MOSFET is [6]-[7]

$$I_{ds} \propto \frac{I_{ds\,0}}{1+\frac{R_{ds} I_{ds\,0}}{V_{dseff}}}, \tag{1}$$

$$I_{ds\,0} \propto \frac{V_{gsteff}\,\mu_{eff} V_{dseff}\left(1-\frac{A_{bulk} V_{dseff}}{2(V_{gsteff}+2V_T)}\right)}{\left(1+\frac{V_{dseff}}{E_{SAT} L_{eff}}\right)}, \tag{2}$$

where I_{ds}, I_{ds0}, R_{ds}, V_{dseff}, V_{gsteff}, A_{bulk}, μ_{eff}, V_T, E_{SAT}, and L_{eff} are the drain current with short-channel effects, drain current of a long channel device, parasitic drain-to-source resistance, effective drain-to-source voltage, effective gate overdrive $(V_{GS}-V_t)$, parameter to model the bulk charge effect, effective carrier mobility, thermal voltage, electric field at which the carrier drift velocity saturates, and effective channel length, respectively.

Threshold voltage, carrier mobility, and saturation velocity are [6]-[7]

$$NMOS: \quad V_t(T) = V_t(T_0) + \left(KT1 + \frac{KT1L}{L_{eff}} + V_{bseff} KT2\right)\left(\frac{T}{T_0}-1\right), \tag{3}$$

$$PMOS: \quad V_t(T) = V_t(T_0) - \left(KT1 + \frac{KT1L}{L_{eff}} + V_{bseff} KT2\right)\left(\frac{T}{T_0}-1\right), \tag{4}$$

$$\mu_{eff}(T) = \left(U_0\left(\frac{T}{T_0}\right)^{U_{te}}\right)\left\{1+\left(\frac{V_{gsteff}+2V_t(T)}{T_{OX}}\right)^2 U_b(T) + (U_c(T) V_{bseff} + U_a(T))\left(\frac{V_{gsteff}+2V_t(T)}{T_{OX}}\right)\right\}^{-1}, \tag{5}$$

$$V_{SAT}(T) = V_{SAT}(T_0) - AT\left(\frac{T}{T_0}-1\right), \tag{6}$$

where V_t, $KT1$, $KT1L$, $KT2$, V_{bseff}, U_0, U_{te}, T_{OX}, U_a, U_b, U_c, V_{SAT}, AT, T_0, and T are the threshold voltage, temperature coefficient for threshold voltage, channel length dependence of the temperature coefficient for threshold voltage, body-bias coefficient of threshold voltage temperature effect, effective substrate bias voltage, mobility at the reference temperature, mobility temperature exponent, gate-oxide thickness, first order mobility degradation coefficient, second order mobility degradation coefficient, body effect of mobility degradation coefficient, saturation velocity, temperature coefficient of saturation velocity, temperature at which the model parameters are extracted, and the operating temperature, respectively. $KT1$, $KT1L$, $KT2$, and AT are temperature independent empirical parameters while U_a, U_b, and U_c are temperature dependent [6]-[7]. U_a, U_b, and U_c are

$$U_a(T) = U_a(T_0) + U_{a1}\left(\frac{T}{T_0}-1\right), \tag{7}$$

$$U_b(T) = U_b(T_0) + U_{b1}\left(\frac{T}{T_0}-1\right), \tag{8}$$

$$U_c(T) = U_c(T_0) + U_{c1}\left(\frac{T}{T_0}-1\right), \tag{9}$$

where U_{a1}, U_{b1}, and U_{c1} are the temperature coefficients of U_a, U_b, and U_c, respectively. As given by (3), (4), (5), and (6), absolute values of threshold voltage, carrier mobility, and saturation velocity degrade as the temperature is increased [6]-[7]. The saturation velocity is typically a weak function of temperature [3]. Threshold voltage degradation with temperature tends to enhance the drain current because of the increase in gate overdrive $(V_{GS}-V_t)$. Alternatively, degradation in carrier mobility tends to lower the drain current as given by (1) and (2). Effective variation of MOSFET drain current is, therefore, determined by the variation of the dominant device parameter when the temperature fluctuates.

3. DEVICE AND CIRCUIT BEHAVIOR UNDER TEMPERATURE FLUCTUATIONS

Influence of temperature fluctuations on device and circuit characteristics is evaluated in this section for TSMC 180nm CMOS technology. The model parameter coefficients that determine the temperature fluctuation induced MOSFET drain current variations are listed in Table I. Gate overdrive and carrier mobility variations due to temperature fluctuations at different supply voltages are listed in Table II.

For circuits operating at the nominal supply voltage (V_{DD} = 1.8V), variations in gate overdrive are smaller as compared to carrier mobility variations when the temperature is increased from 25°C to 125°C. The MOSFET drain current and the circuit speed are, therefore, reduced following the degradation of carrier mobility as the temperature is increased. Propagation delay variations of various circuits with temperature at the nominal supply voltage are shown in Fig. 2. When operating at the nominal supply voltage, the speed of circuits degrade by up to 19.6% as the temperature is increased from 25°C to 125°C.

4. SUPPLY VOLTAGE OPTIMIZATION

The results presented in Section 3 indicate that operating an integrated circuit at the prescribed nominal supply voltage is not

preferable for reliable circuit operation under temperature fluctuations. A design methodology based on scaling the supply voltage for suppressing the drain current variations due to temperature fluctuations is described in [2], [9], and [13]. In order to compensate for the variation of carrier mobility, the sensitivity of gate overdrive to temperature fluctuations should be enhanced by lowering the supply voltage [2]. At the optimum supply voltage, the temperature fluctuation induced gate overdrive variation completely counterbalances the carrier mobility variation [2]. A transistor biased at this optimum supply voltage produces a temperature variation insensitive constant drain current, as illustrated in Fig. 1.

TABLE I
MODEL PARAMETER COEFFICIENTS THAT EFFECT THE MOSFET DRAIN CURRENT AS THE TEMPERATURE FLUCTUATES

Model Parameters	**PMOS**	**NMOS**
KT1	-0.214	-0.196
KT1L	0	0
KT2	-0.035	-0.039
U_{te}	-0.599	-1.945
U_{a1}	1.22E-09	1.22E-09
U_{b1}	-1.44E-18	-3.08E-18
U_{c1}	1.97E-10	-2.39E-10
AT	10000	20000

TABLE II
GATE OVERDRIVE AND CARRIER MOBILITY VARIATIONS AT DIFFERENT SUPPLY VOLTAGES

Supply Voltage (V)	Temperature (°C)	Gate Overdrive (V)		Carrier Mobility ($x10^{-3}$ m^2/Vs)	
		PMOS	NMOS	PMOS	NMOS
1.8	25	-1.34	1.33	5.46	28.86
	125	-1.41	1.39	4.47	17.93
	Variation (%)	5.37	4.95	-18.26	-37.87
1.1	25	-0.64	0.63	6.31	35.10
	125	-0.71	0.69	5.13	20.08
	Variation (%)	11.28	10.48	-18.69	-42.78
0.7	25	-0.24	0.23	6.98	37.78
	125	-0.31	0.29	5.70	20.95
	Variation (%)	30.39	29.01	-18.36	-44.54
0.5	25	-0.04	0.03	7.39	38.66
	125	-0.11	0.09	6.06	21.25
	Variation (%)	198.88	249.31	-17.98	-45.03

As listed in Table II, the gate overdrive variations at the nominal supply voltage (V_{DD} = 1.8V) are similar for n-channel and p-channel devices. Alternatively, temperature fluctuation induced variations in the electron mobility of an NMOS transistor are higher as compared to the hole mobility variations of a PMOS transistor. The supply voltage should, therefore, be scaled to a lower value in an NMOS device as compared to a PMOS device to be able to compensate the mobility variations for achieving temperature variation insensitive drain current as shown in Fig. 1.

The optimum supply voltages for various test circuits in a 180nm CMOS technology are presented in Fig. 3. Circuits display a temperature variation insensitive performance when operated at a supply voltage 45% to 53% lower than the nominal supply voltage (V_{DD} = 1.8V). The optimum supply voltage of each CMOS circuit is within the range of the optimum supply voltages of the individual n-channel and p-channel devices, as shown in Figs. 1 and 3.

5. OPTIMIZATION FOR MINIMUM ENERGY-DELAY PRODUCT

The results presented in Section 4 indicate that there is an optimum supply voltage at which the speed characteristics of an integrated circuit is insensitive to temperature fluctuations. The supply voltage that achieves temperature variation insensitive circuit performance is lower than the nominal supply voltage (V_{DD} = 1.8V) in a 180nm CMOS technology. Integrated circuits operating at scaled supply voltages consume low power at the cost of reduced speed. The design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance is, therefore, particularly attractive in low power applications with relaxed speed requirements.

Low power designs aim at reducing power, power-delay product, or energy-delay product [5], [8], [10], [11]. Energy-delay product metric provides a good compromise between the need to reduce energy consumption and the requirement to operate the circuits at an appropriate speed [5]. The energy-delay product is [5], [11], [14]

$$EDP \approx \sum_{j} C_{eff,j} V_{DD}^2 T_g + \sum_{j} \sum_{j_i} I_{leak,j_i} V_{DD} T_g T_c, \quad (10)$$

$$I_{leak,j_i} = \frac{\mu_{j_i} W_{j_i} C_{OX}}{L_{eff}} V_{T,j_i}^2 e^{\frac{|V_{GS,j_i}| - |V_{t,j_i}|}{n_{j_i} V_{T,j_i}}} \left(1 - e^{\frac{-|V_{DS,j_i}|}{V_{T,j_i}}}\right), \quad (11)$$

where EDP, V_{DD}, T_g, T_c, μ, W, C_{OX}, L_{eff}, V_t, V_T, V_{GS}, V_{DS}, and n are energy-delay product, supply voltage, propagation delay of the circuit, clock period, carrier mobility, transistor width, oxide capacitance per unit area, effective channel length, threshold voltage, thermal voltage, gate-to-source voltage, drain-to-source voltage, and subthreshold swing coefficient, respectively. C_{eff} is the average effective switched capacitance of each gate that is extracted to include the average activity factor and the energy consumed due to short circuit current and glitches. The indices j and i cover all the gates in the circuit and all the transistors that produce net subthreshold leakage current in each gate, respectively.

The normalized energy per cycle, delay, and energy-delay product as a function of the supply voltage at the room temperature (25°C) for an inverter in a 180nm CMOS technology is shown in Fig. 4. As the supply voltage is reduced, the energy per cycle decreases while the propagation delay increases [5]-[8]. The energy-delay product, therefore, has a minimum as shown in Fig. 4.

Energy per cycle and propagation delay are also dependent on the die temperature [9]-[10]. As the temperature increases, energy consumed by a circuit increases primarily due to the increase in subthreshold leakage current [14]. Similarly, the propagation delay of circuits in current CMOS technologies increase when the temperature is increased at the nominal supply voltage, primarily due to the degradation in carrier mobility as explained in Sections 2 and 3. Circuits that operate close to the nominal supply voltage, therefore, display the worst case energy-delay product at the maximum temperature for which the circuit is functional.

Speed characteristics of circuits are also dependent on the supply voltage [2]. As listed in Table II, scaling the supply voltage enhances

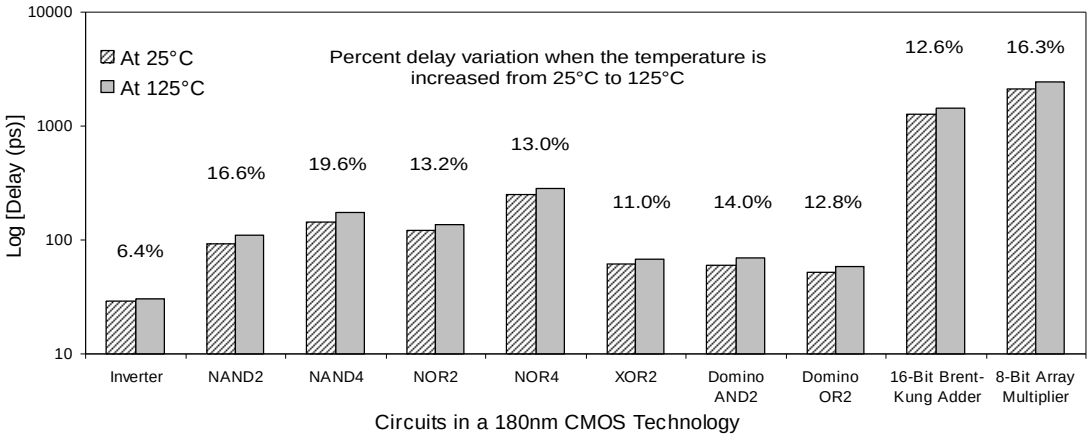

Fig. 2. Percent delay variation with temperature for circuits operating at the nominal supply voltage (V_{DD} = 1.8V) in a 180nm CMOS technology.

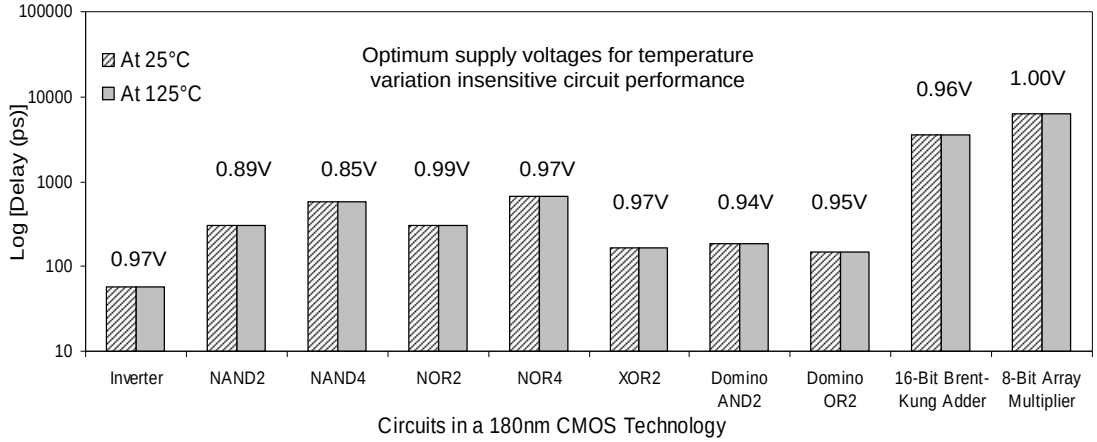

Fig. 3. Optimum supply voltages that achieve temperature variation insensitive speed characteristics in a 180nm CMOS technology.

the sensitivity of gate-overdrive to temperature variations. At supply voltages below the optimum supply voltage, the gate overdrive variations dominate the carrier mobility variations when the temperature fluctuates. The MOSFET drain current and the circuit speed are, therefore, enhanced when the temperature is increased at supply voltages below the optimum supply voltage.

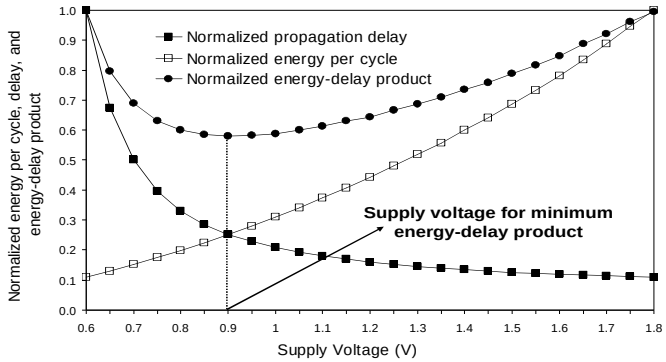

Fig. 4. Normalized energy per cycle, delay, and energy-delay product as a function of the supply voltage at the room temperature (25°C) for an inverter.

Energy-delay product at two different temperatures and percent delay variation when the temperature is increased from 25°C to 125°C are presented as a function of supply voltage for an 8-bit array multiplier in Fig. 5. For the supply voltages above the optimum supply voltage, delay variations are determined primarily by the mobility variations. As listed in Table II, the percent variation in carrier mobility is similar for a specific temperature range at different supply voltages. Alternatively, the sensitivity of gate overdrive to temperature variations is enhanced with the scaling of supply voltage. Therefore, as the supply voltage is scaled below the optimum supply voltage, the rate of increase of delay variations (determined primarily by the variations of the gate overdrive for $V_{DD} < V_{Optimum}$) is enhanced as shown in Fig. 5.

Due to the higher rate of delay variations below the optimum supply voltage, reduction in the propagation delay dominates the increase in energy in the EDP term as the temperature is increased. The energy-delay product at 25°C is, therefore, higher than the energy-delay product at 125°C for the supply voltages below the optimum supply voltage, as illustrated in Fig. 5. Consequently, the worst case energy-delay product is exhibited at a lower temperature for circuits operating at supply voltages below the optimum supply voltage.

The delay, energy-delay product, and delay variations for circuits operating at the nominal supply voltage, supply voltage for temperature variation insensitive delay, and the supply voltage for minimum energy-delay product are listed in Table III. The delay and the energy-delay product of a circuit at different supply voltages are normalized to delay and energy-delay product of the corresponding circuit at the room temperature (25°C) and the nominal supply voltage (V_{DD} = 1.8V). As shown in Fig. 5 and listed in Table III, the

supply voltages that achieve minimum energy-delay product are comparable to the supply voltages that achieve temperature variation insensitive speed. The variation in circuit speed is up to 9.6% when the temperature is increased from 25°C to 125°C at the supply voltages providing minimum energy-delay product.

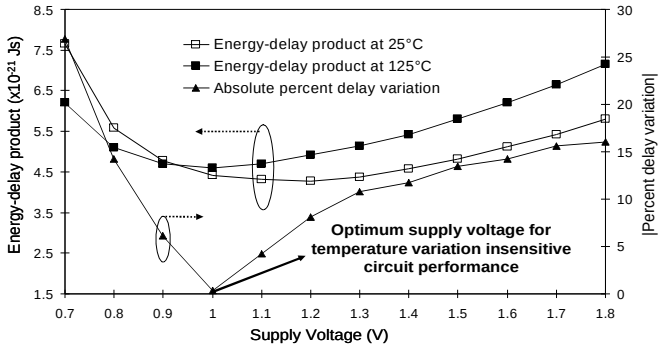

Fig. 5. The energy-delay product at two different temperatures and the percent delay variation as a function of the supply voltage. The temperature is increased from 25°C to 125°C for an 8-bit array multiplier.

6. TEMPERATURE VARIATION INSENSITIVE LOW POWER CMOS CIRCUITS

The tradeoffs of operating the circuits at the supply voltages providing temperature variation insensitive circuit performance are discussed in this section. The energy, delay, and energy-delay product (EDP) at the supply voltages that yield temperature variation insensitive circuit performance and minimum energy-delay product are compared.

At the supply voltages for minimum energy-delay product, the energy per cycle is 59% to 82% lower than the energy per cycle at the nominal supply voltage (V_{DD} = 1.8V). Similarly, the energy per cycle at the optimum supply voltages that yield temperature variation insensitive circuit performance is 71% to 81% lower than the energy per cycle at the nominal supply voltage. The circuit speed, as compared to the speed at the nominal supply voltage, degrades by up to 206% and 224% when the circuits are operated at the supply voltages for minimum energy-delay product (V_{DD} optimized for minimum EDP at 125°C) and temperature variation insensitive circuit performance, respectively.

The minimum energy-delay product is 23% to 47% lower than the energy-delay product at the nominal supply voltage (V_{DD} = 1.8V). Similarly, the energy-delay product at the optimum supply voltages that yield temperature variation insensitive circuit performance is 20% to 45% lower than the energy-delay product at the nominal supply voltage. The difference of the minimum achievable energy-delay product and the energy-delay product at the supply voltages for temperature variation insensitive circuit performance is less than 6%. Low-power integrated circuits can, therefore, also be made insensitive to temperature fluctuations with a modest amount of increase in energy-delay product.

7. CONCLUSIONS

A design methodology for temperature variation insensitive low power circuits in a 180nm CMOS technology is presented in this paper. Temperature dependent device parameters that cause variations in MOSFET drain current are identified. When operating at the nominal supply voltage, the speed of circuits degrade by up to 19.6% as the temperature is increased from 25°C to 125°C. Operating an integrated circuit at the prescribed nominal supply voltage is not preferable for reliable circuit operation under temperature fluctuations. Circuits display a temperature variation insensitive performance when operated at a supply voltage 45% to 53% lower than the nominal supply voltage (V_{DD} = 1.8V). Integrated circuits operating at scaled supply voltages consume low power at the cost of reduced performance. The design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance is, therefore, particularly attractive in low power applications with relaxed speed requirements.

The energy-delay product at the optimum supply voltages that yield temperature variation insensitive circuit performance is 20% to 45% lower than the energy-delay product at the nominal supply voltage. The energy-delay product at the optimum supply voltages is within 6% of the minimum achievable energy-delay product. Low-power integrated circuits can therefore be made insensitive to temperature fluctuations by considering the temperature fluctuations in the voltage optimization process. The optimum supply voltages are similar for a diverse set of circuits. The proposed technique of operating large scale designs at a supply voltage close to the optimum supply voltage for temperature variation insensitive low power circuits is, therefore, feasible.

REFERENCES

[1] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, "Parameter Variation and Impact on Circuits and Microarchitecture," *Proceedings of the IEEE/ACM International Design Automation Conference*, pp. 338-342, June 2003.

[2] R. Kumar and V. Kursun, "Voltage Optimization for Temperature Variation Insensitive CMOS Circuits," *Proceedings of the IEE International Midwest Symposium on Circuits and Systems*, pp. 476-479, August 2005.

[3] Y. Cheng, K. Imai, M. C. Jeng, Z. Liu, K. Chen, and C. Hu, "Modeling Temperature Effects of Quarter Micrometre MOSFET in BSIM3v3 for Circuit Simulation," *Semiconductor Science Technology*, Vol. 12, pp. 1349-1354, November 1997.

[4] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill, New York, 1999.

[5] M. R. Stan, "Optimal Voltages and Sizing for Low Power," *Proceedings of the IEEE International Conference on VLSI Design*, pp. 428-433, January 1999.

[6] W. Liu *et al.*, *BSIM3v3.2.2 MOSFET Model – User Manual*, Department of Electrical and Computer Engineering, University of California, Berkeley, 1999.

[7] Y. Cao, T. Sato, D. Sylvester, M. Orshansky, and C. Hu, "New Paradigm of Predictive MOSFET and Interconnect Modeling for Early Circuit Design," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 201-204, June 2000.

[8] M. Horowitz, T. Indermaur, and R. Gonzalez, "Low-power Digital Design," *Proceedings of the IEEE International Symposium of Low Power Electronics and Design*, pp. 8-11, October 1994.

[9] A. Bellaouar, A. Fridi, M. J. Elmasry, and K. Itoh, "Supply Voltage Scaling for Temperature Insensitive CMOS Circuit Operation," *IEEE Transactions on Circuits and Systems II*, Vol. 45, No. 3, pp. 415-417, March 1998.

[10] B. H. Calhoun, A. Wang, and A. Chandrakasan, "Modeling and Sizing for Minimum Energy Operation in Subthreshold Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 9, pp. 1778-1786, September 2005.

TABLE III
NORMALIZED DELAY, ENERGY-DELAY PRODUCT, AND DELAY VARIATIONS AT THE NOMINAL SUPPLY VOLTAGE, SUPPLY VOLTAGE FOR TEMPERATURE VARIATION INSENSITIVE DELAY, AND THE SUPPLY VOLTAGE FOR MINIMUM ENERGY-DELAY PRODUCT FOR CIRCUITS IN A 180NM CMOS TECHNOLOGY

180nm CMOS Technology		Temp (°C)	Inverter	NAND2	NAND4	NOR2	NOR4	XOR2	Domino AND2	Domino OR2	16-Bit Brent-Kung Adder	8-Bit Array Multiplier
Nominal Supply Voltage V_{DD} = 1.8V	Delay	25	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
		125	1.06	1.17	1.20	1.13	1.13	1.11	1.14	1.13	1.13	1.16
	EDP	25	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
		125	1.07	1.18	1.22	1.15	1.15	1.11	1.16	1.15	1.15	1.23
	Delay Variation (%)		6.4	16.6	19.5	13.2	13.0	11.0	14.0	12.8	12.6	16.3
Supply Voltage Optimized for Temperature Variation Insensitive Delay	Supply Voltage (V)		0.97	0.89	0.85	0.99	0.97	0.97	0.94	0.95	0.96	1.00
	Delay	25	2.01	3.24	3.98	2.49	2.65	2.73	3.03	2.84	2.74	2.98
		125	2.01	3.24	4.00	2.50	2.66	2.72	3.04	2.84	2.74	2.98
	EDP	25	0.59	0.67	0.74	0.64	0.63	0.80	0.72	0.72	0.73	0.78
		125	0.59	0.68	0.76	0.66	0.65	0.79	0.73	0.72	0.73	0.81
	Delay Variation (%)		0.1	0.1	0.5	0.2	0.1	-0.1	0.3	0.0	0.0	-0.2
Supply Voltage Optimized for Minimum Energy-Delay Product at 25°C	Supply Voltage (V)		0.91	1.01	1.03	0.99	0.96	1.15	1.06	1.09	1.07	1.16
	Delay	25	2.26	2.35	2.39	2.49	2.72	1.88	2.26	2.06	2.14	2.09
		125	2.23	2.50	2.62	2.50	2.71	1.98	2.37	2.17	2.23	2.22
	EDP	25	0.58	0.65	0.69	0.64	0.63	0.77	0.71	0.70	0.71	0.75
		125	0.57	0.70	0.77	0.66	0.65	0.81	0.75	0.74	0.75	0.84
	Delay Variation (%)		-1.6	6.1	9.6	0.2	-0.2	5.4	5.1	5.5	4.2	6.2
Supply Voltage Optimized for Minimum Energy-Delay Product at 125°C	Supply Voltage (V)		0.82	0.89	0.90	0.85	0.87	1.02	0.93	0.94	0.92	1.01
	Delay	25	2.85	3.24	3.36	3.76	3.55	2.42	3.13	2.92	3.05	2.90
		125	2.69	3.24	3.48	3.46	3.35	2.46	3.12	2.90	2.99	2.91
	EDP	25	0.60	0.67	0.71	0.68	0.64	0.78	0.73	0.73	0.74	0.77
		125	0.56	0.68	0.75	0.64	0.64	0.79	0.73	0.72	0.73	0.81
	Delay Variation (%)		-5.5	0.1	3.7	-8.1	-5.7	1.8	-0.4	-0.5	-2.0	0.3

[11] R. Gonzalez, B. Gordon, and M. Horowitz, "Supply and Threshold Voltage Scaling for Low Power CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 8, pp.1210-1216, August 1997.

[12] R. W. Johnson *et al.*, "The Changing Automotive Environment: High Temperature Electronics," *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 27, No. 3, pp. 164-176, July 2004.

[13] I. M. Filanovsky and A. Allam, "Mutual Compensation of Mobility and Threshold Voltage Temperature Effects with Applications in CMOS Circuits," *IEEE Transactions on Circuits and Systems I*, Vol. 48, No. 7, pp. 876-884, July 2001.

[14] V. Kursun, *Supply and Threshold Voltage Scaling Techniques in CMOS Circuits*, Ph.D. Thesis, Department of Electrical and Computer Engineering, University of Rochester, 2004.