Abstract

The generation, distribution, and dissipation of power are at the forefront of problems faced in the development of high performance integrated circuits. Several techniques for designing low power and high speed integrated circuits are presented in this dissertation. Supply and threshold voltage scaling techniques, targeting lower power consumption and enhanced device reliability without degrading circuit speed, are described.

Systems with multiple supply voltages can significantly reduce power consumption without degrading speed by selectively lowering the supply voltages along non-critical delay paths. High frequency monolithic DC-DC conversion techniques applicable to multiple supply voltage CMOS circuits are presented in order to provide additional voltage levels with low energy and area overhead. Full integration of a high efficiency buck converter on the same die as a dual supply voltage microprocessor is demonstrated to be feasible. A low swing DC-DC conversion technique is presented that enhances the energy efficiency of a monolithic DC-DC converter. Device reliability issues in monolithic DC-DC converters operating at high input voltages are discussed. A cascode bridge circuit that guarantees the reliable operation of deep submicrometer MOSFETs without exposure to high voltage stress while operating at high input and output voltages is introduced.

An important technique for reducing the impact of supply voltage scaling on circuit performance is scaling threshold voltages. Exponentially increasing subthreshold leakage currents and worsening short-channel effects at reduced threshold voltages are discussed. Increasing performance degradation caused by die-to-die and within-die parameter variations at reduced gate lengths and threshold voltages is described. Dynamic threshold voltage scaling techniques reduce the deleterious effects of static threshold voltage scaling. A novel variable threshold voltage CMOS circuit technique for simultaneously enhancing the speed and power

characteristics of dynamic circuits is presented. Both reverse and forward body bias techniques are applied to domino logic circuits for enhanced robustness against on-chip noise. Multiple threshold voltage CMOS circuits offer decreased subthreshold leakage currents and enhanced performance by selectively lowering the threshold voltages along the speed critical paths. A sleep switch dual threshold voltage domino logic circuit technique providing significant savings in subthreshold leakage energy is described.